Decoding and Synthesizing Transformerless PWM Converters

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- Resonance is the main principle of high-efficiency power transfer.
- **Converters were evolved and deduced from the original converter, buck converter.**
- Hopefully, no more trial and error in synthesizing PMW Converters.

I. Introduction

➢ Six PWM Converters

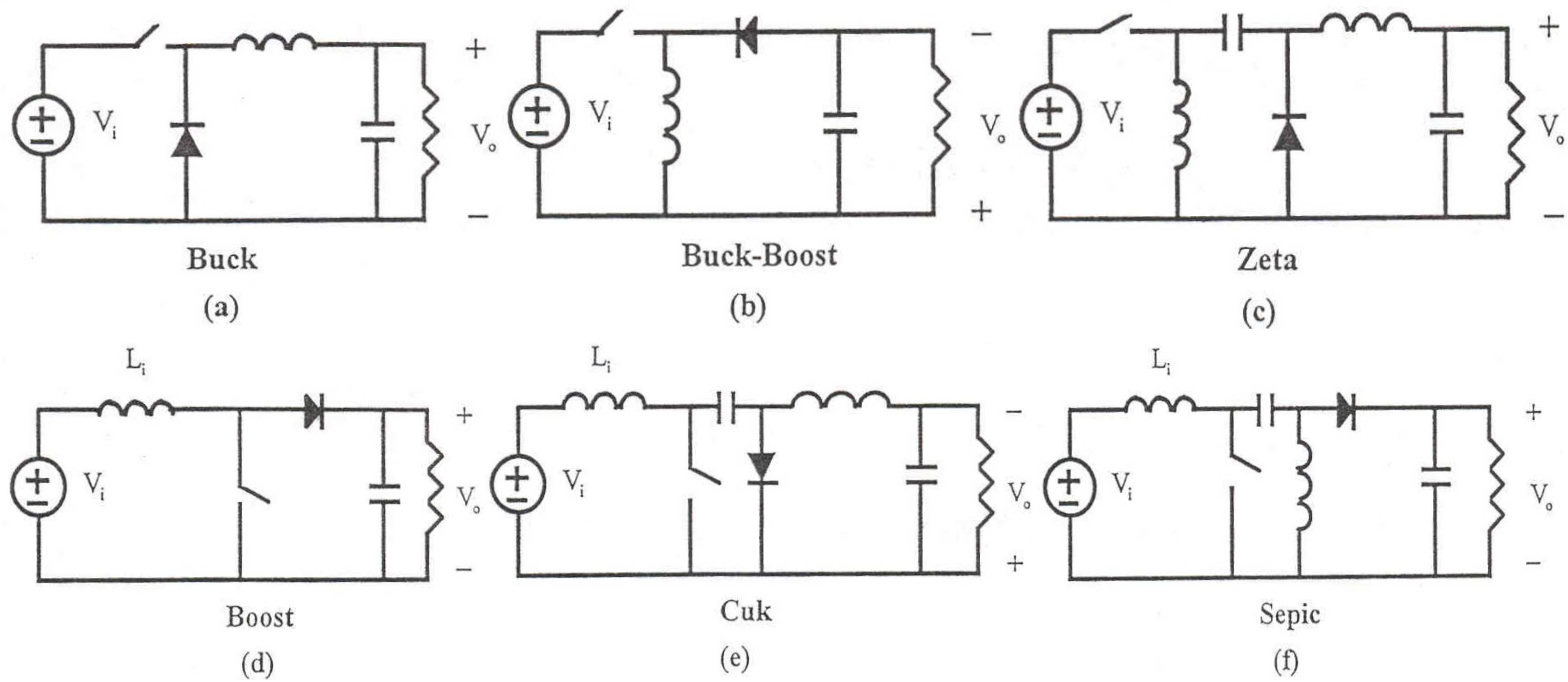
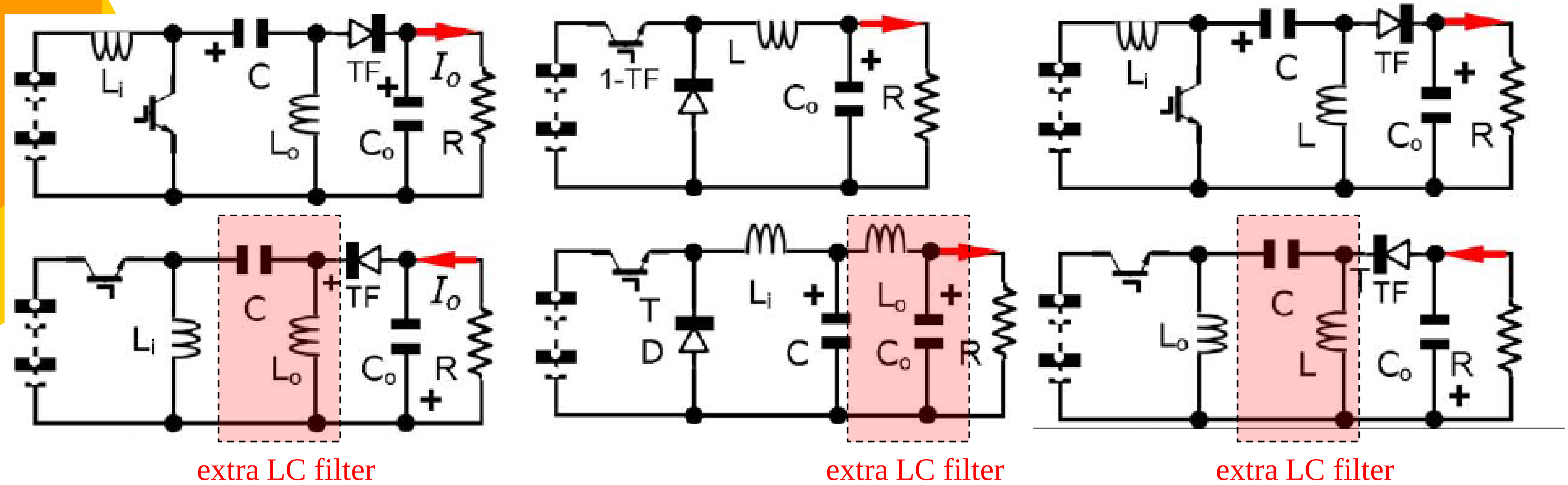


Fig. 1.

➢ Six-PWM-Converter Derived Converters



(a) (b) (c)

Fig. 2.

➢ Switched Cap./Ind. Hybrid Converters

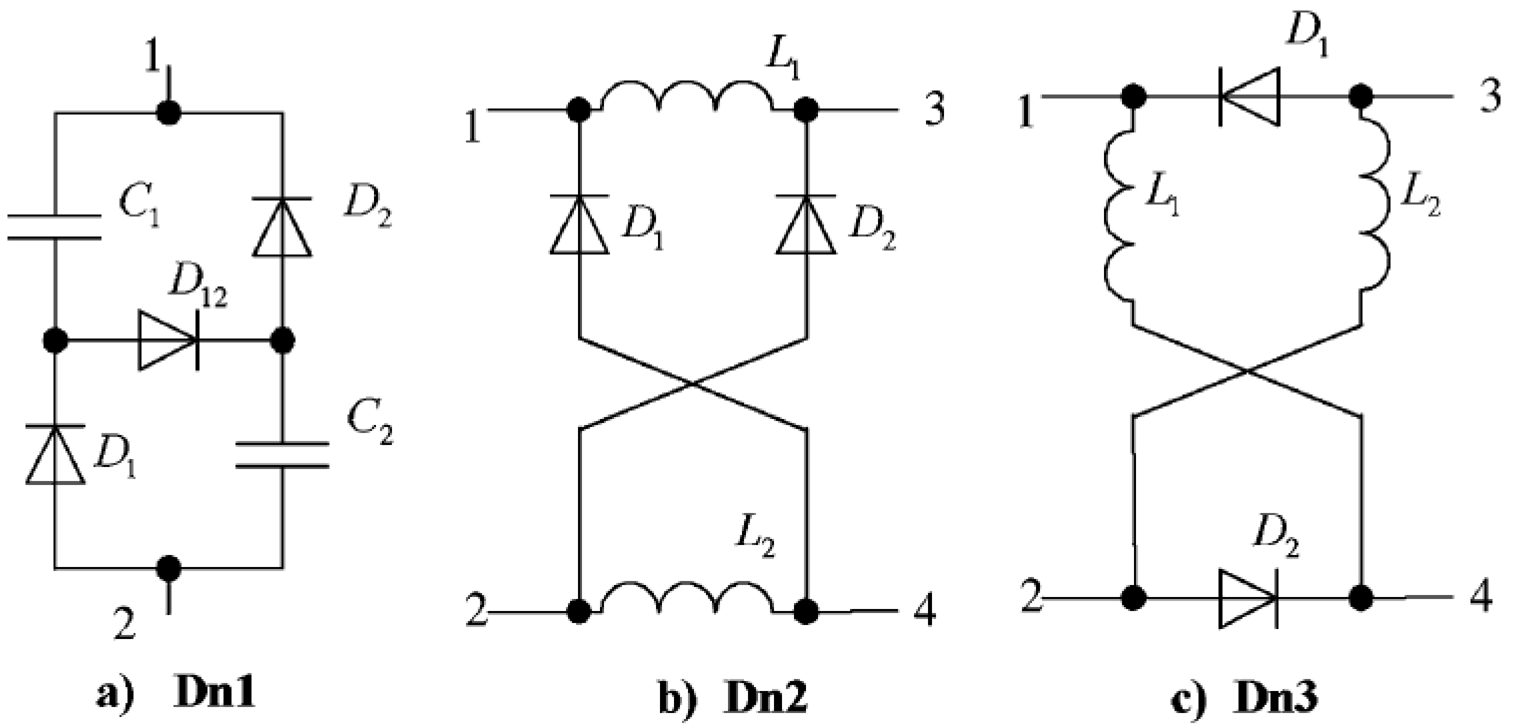


Fig. 3. Step-down basic switching structures.

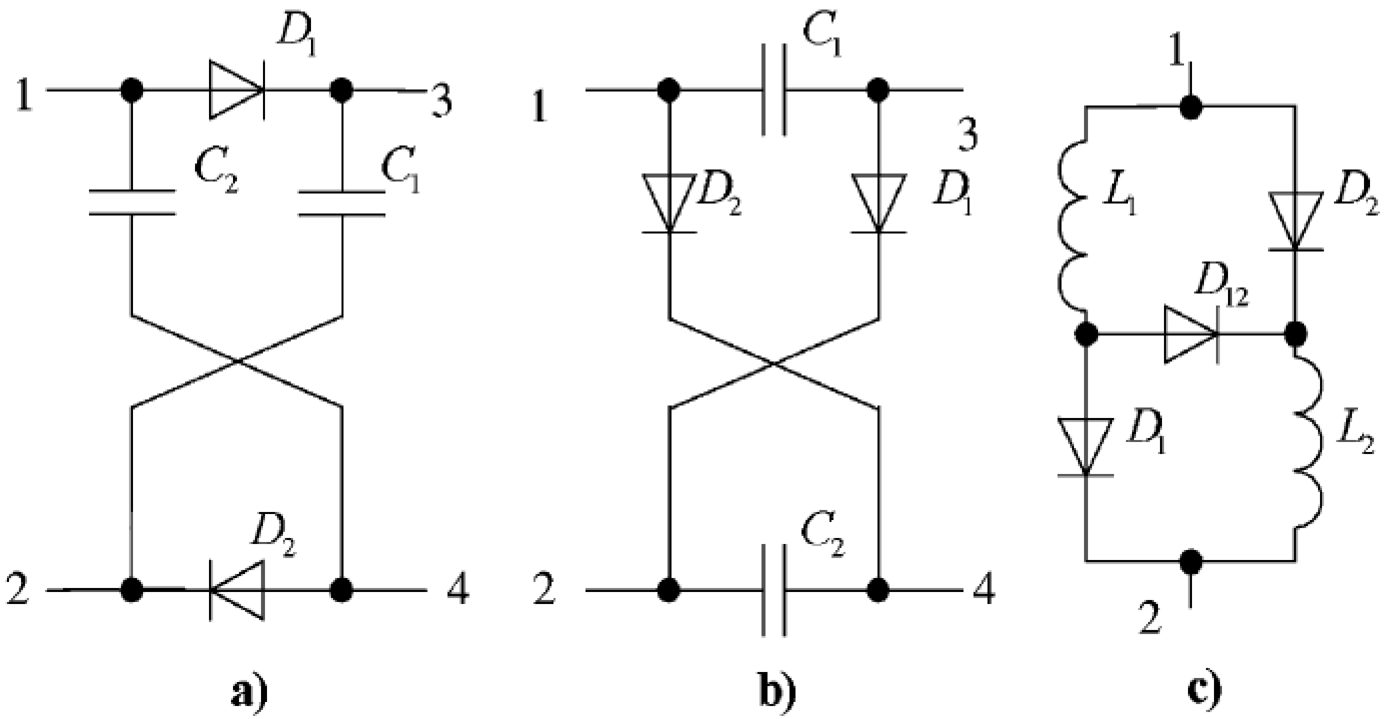


Fig. 4. Step-up basic switching structures. (a) Up1. (b) Up2. (c) Up3.

TABLE I

POSSIBLE REALIZATIONS OF HYBRID CONVERTERS WITH *C*-/*L*-SWITCHING STRUCTURES

C/L-switching struc / Converter	Dn1	Dn2	Dn3	Up1	Up2	Up3
Buck	✸	✸				
Boost				✸		✸
Buck- Boost	✸			✸		✸
Ćuk	✸	✸			✸	✸
Sepic	✸		✸			✸
Zeta		✸			✸	✸

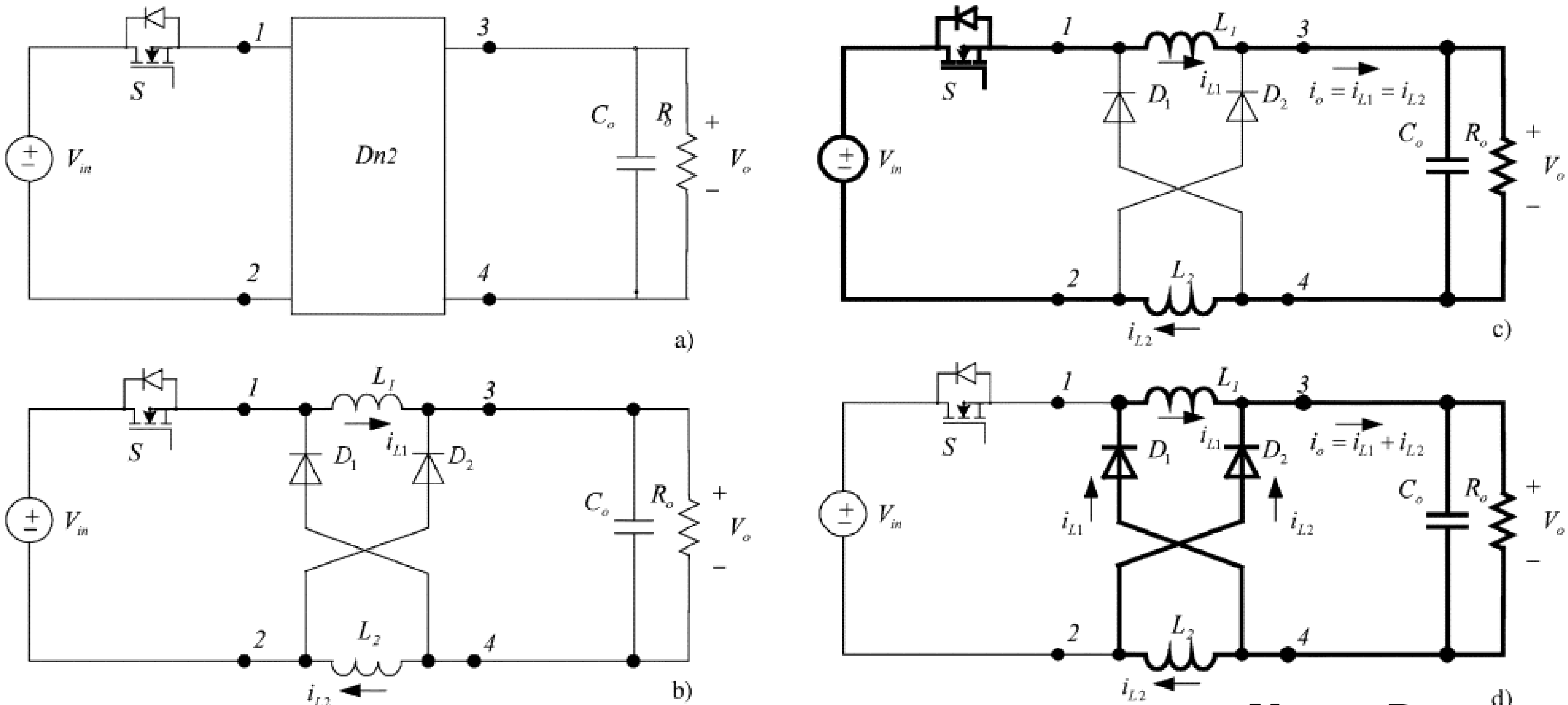


Fig. 5.

$$\frac{V_O}{V_{in}} = \frac{D}{2-D}$$

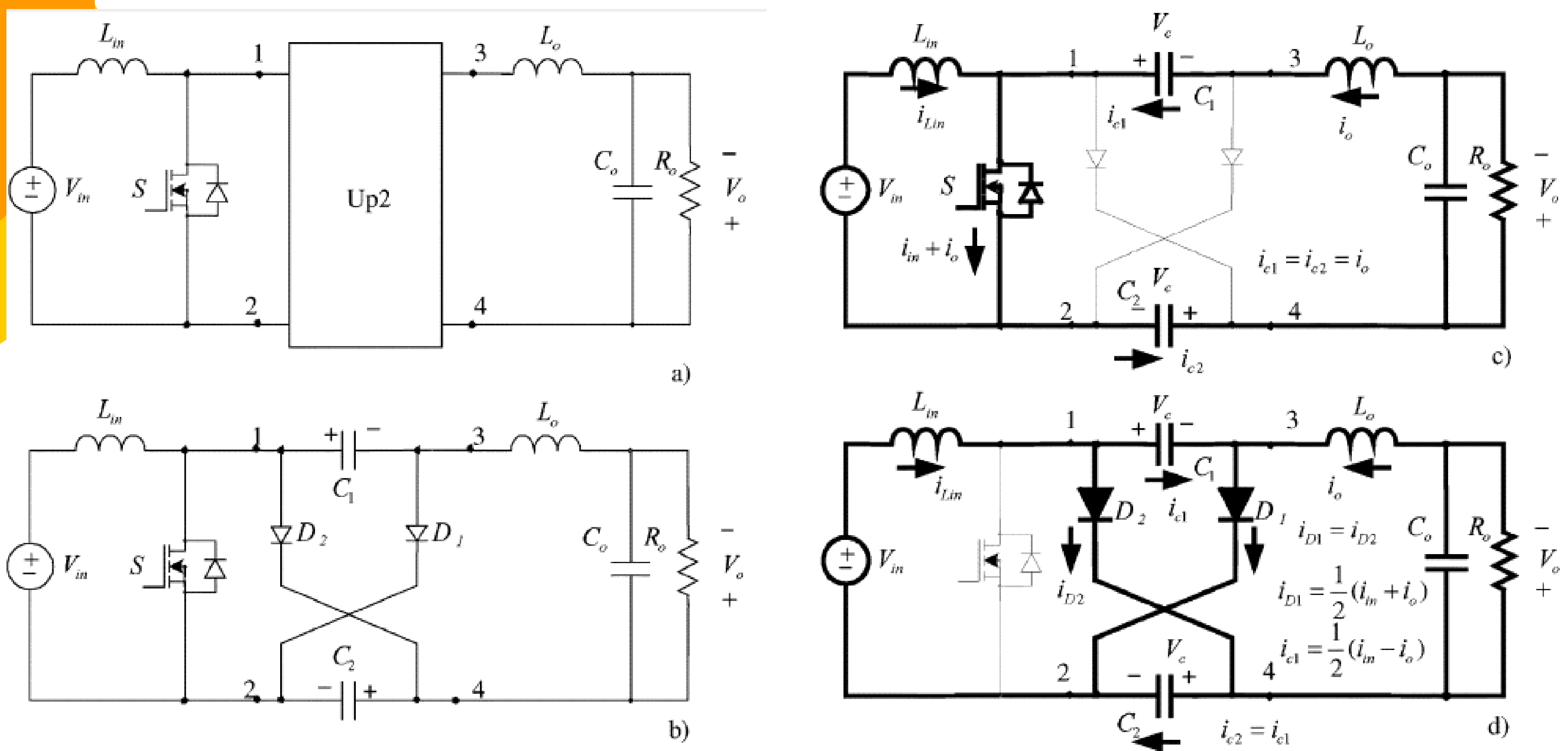
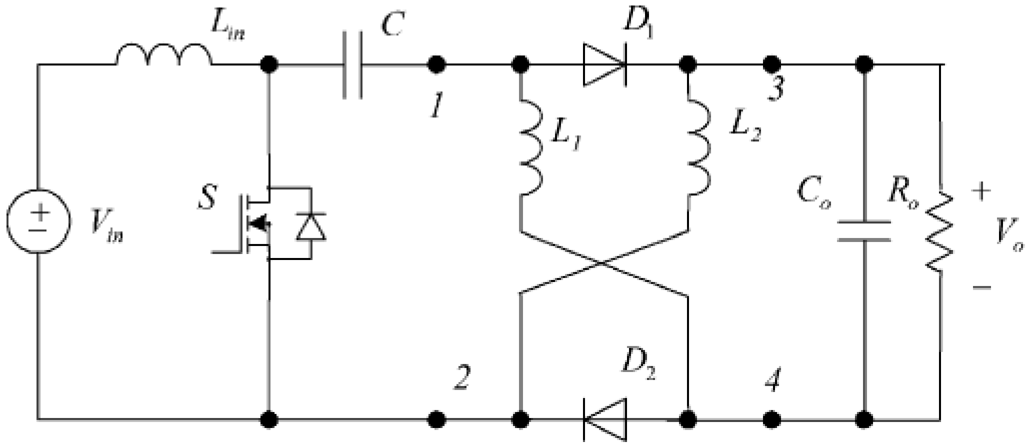


Fig. 6.

$$\frac{V_O}{V_{in}}=\frac{1+D}{1-D}$$



$$\frac{V_O}{V_{in}} = \frac{D}{2(1-D)}$$

Fig. 7.

➢ Single-Stage Converters

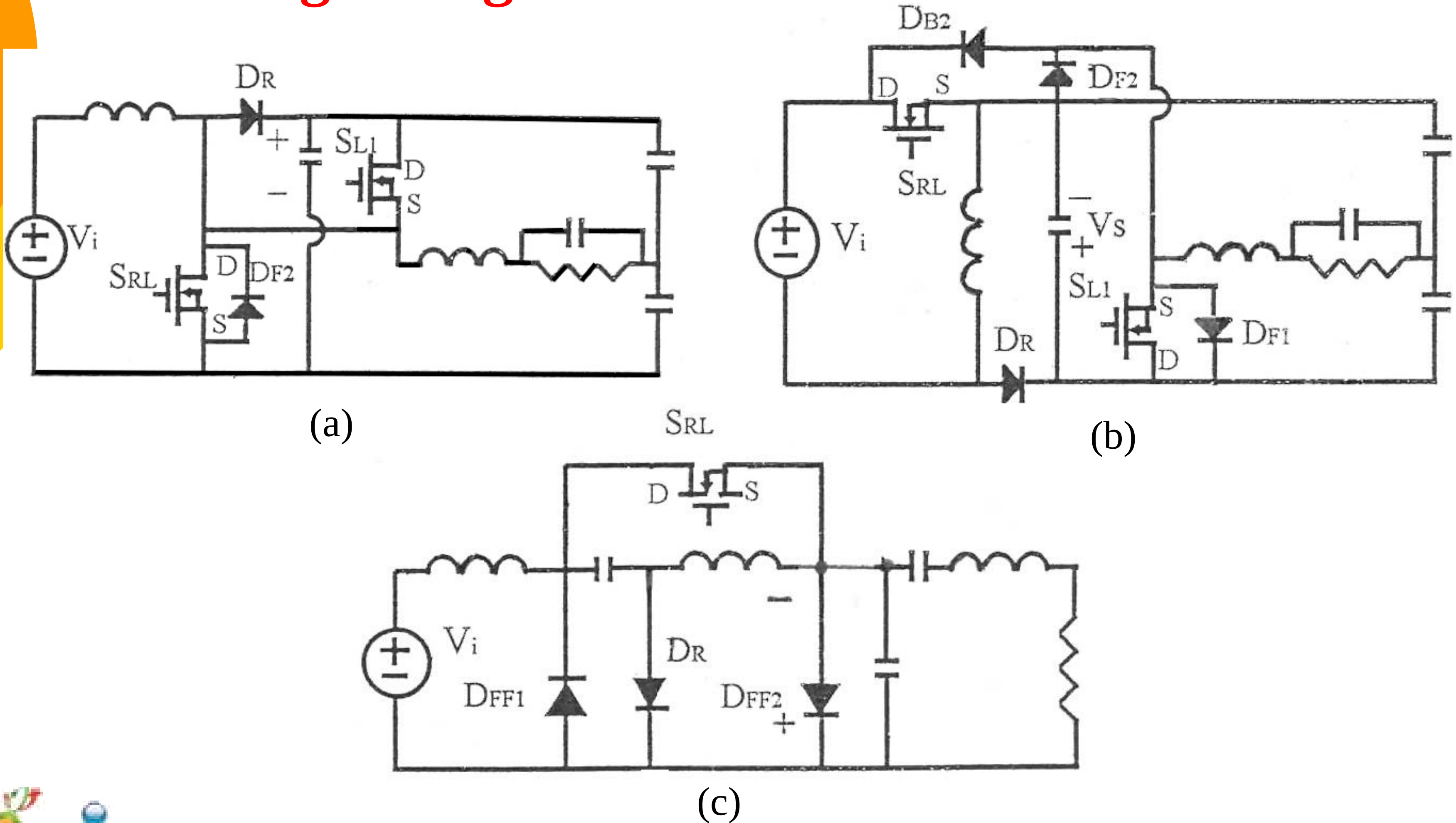
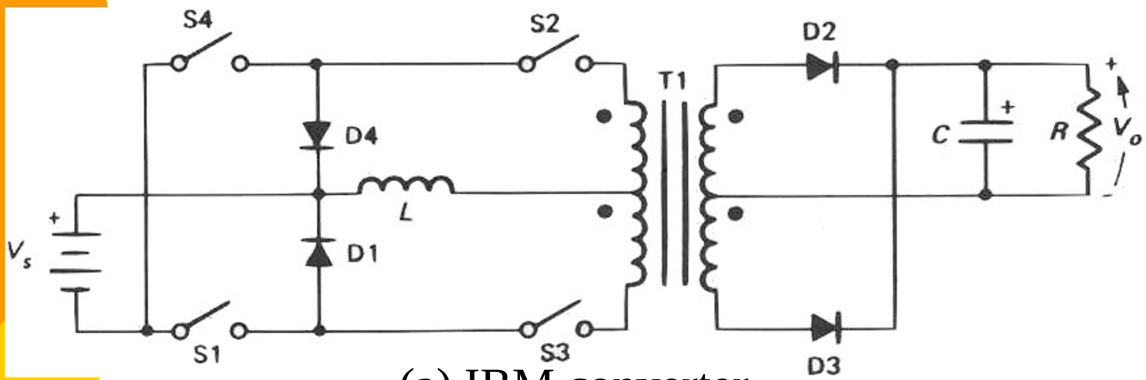
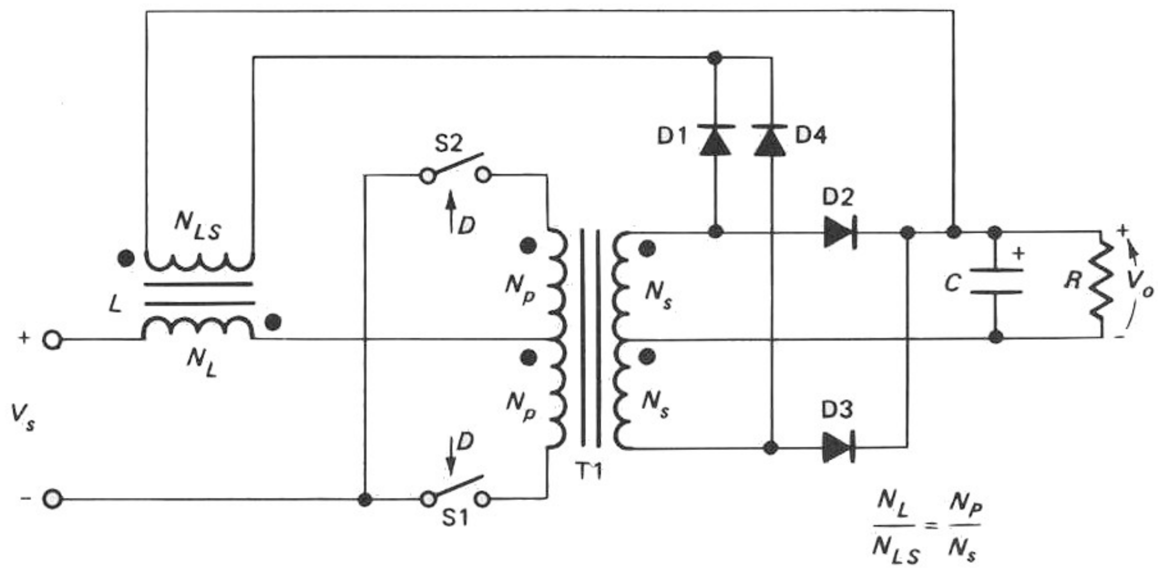


Fig. 8.

➢ Buck Derived PWM Converters



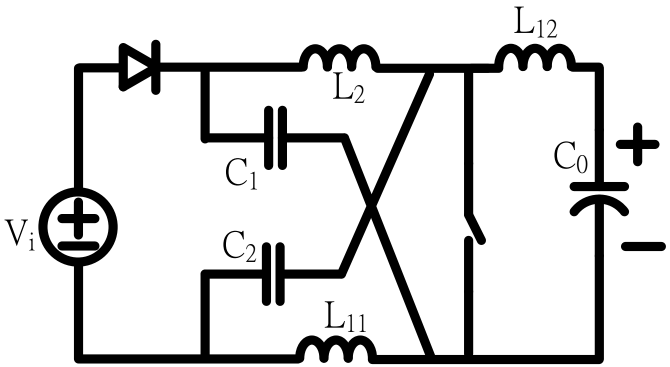
(a) IBM converter



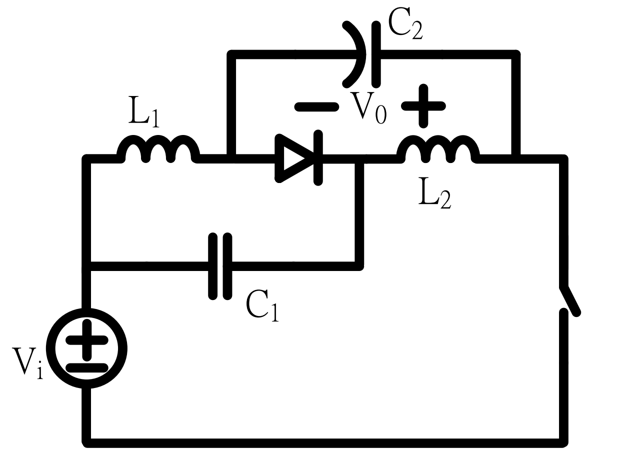
(b) Improved Weinberg converter

Fig. 9.

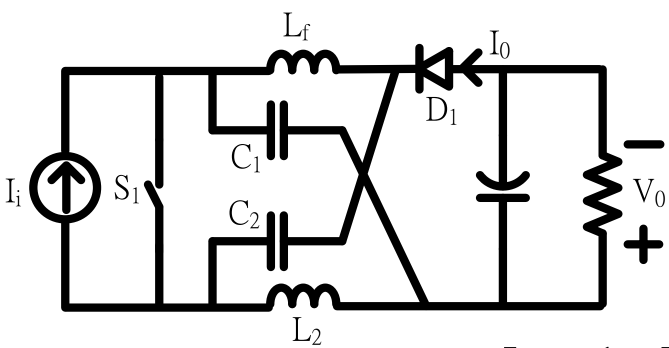
➢ Z-source Converters



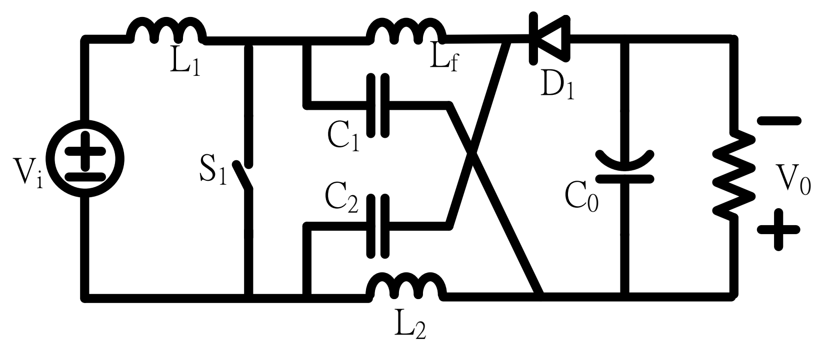
(a) Voltage-fed Z-source $\frac{V_0}{V_i}=\frac{1-D}{1-2D}$



(b) Quasi Z-source $\frac{V_0}{V_i}=\frac{D}{1-2D}$



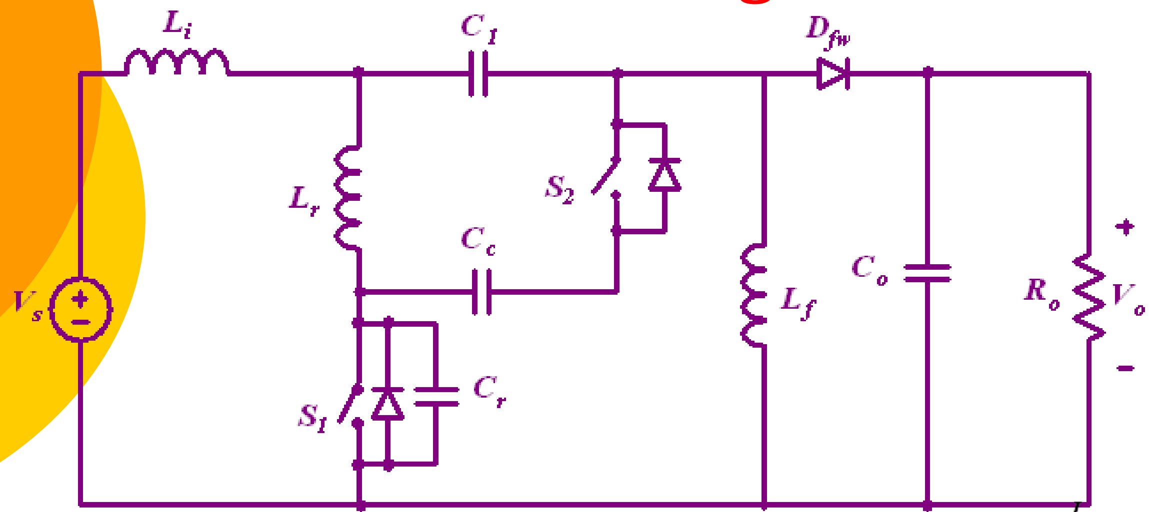
(c) Current-fed Z-source $\frac{I_0}{I_i}=\frac{1-D}{2D-1}$



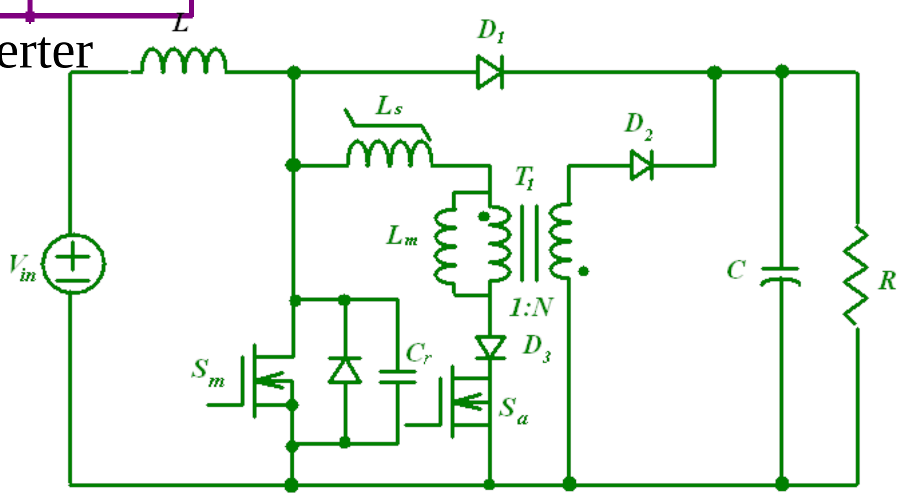
$$\frac{V_0}{V_i}=\frac{2D-1}{1-D}$$

Fig. 10.

➢ Soft Switching PWM Converters



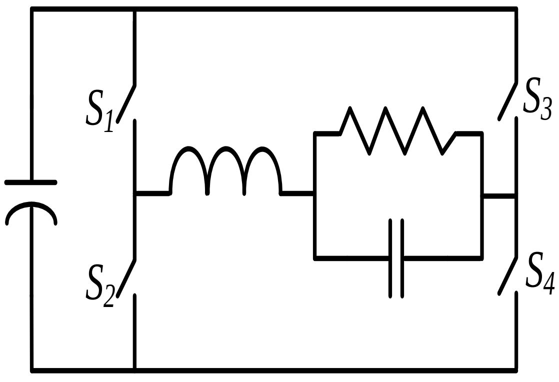
Active soft-switching SEPIC converter



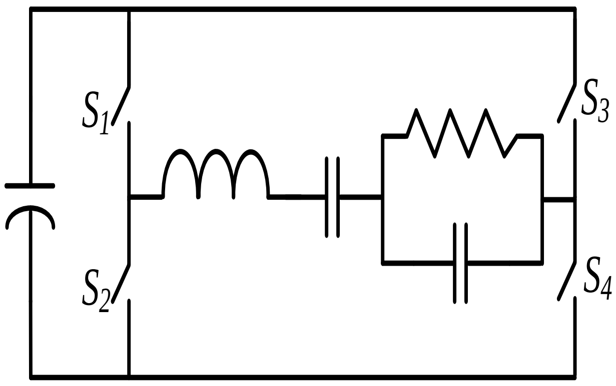
Boost + flyback

Fig. 11.

➢ Resonant Converters



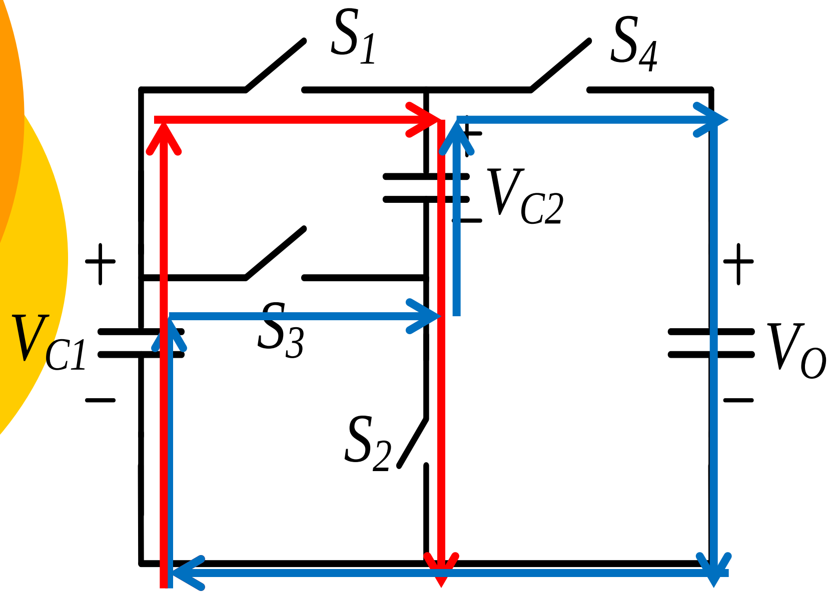
(a) Series-Parallel



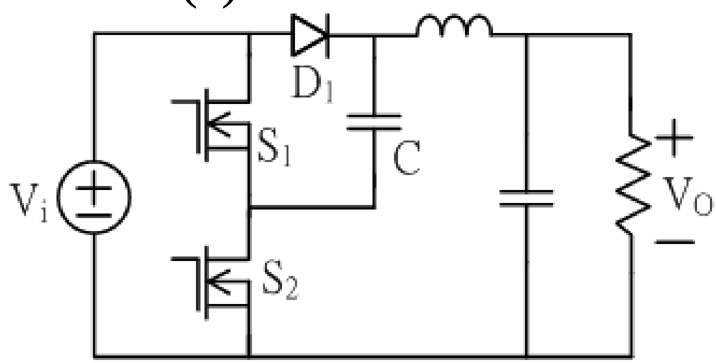
(b) LCC

Fig. 12.

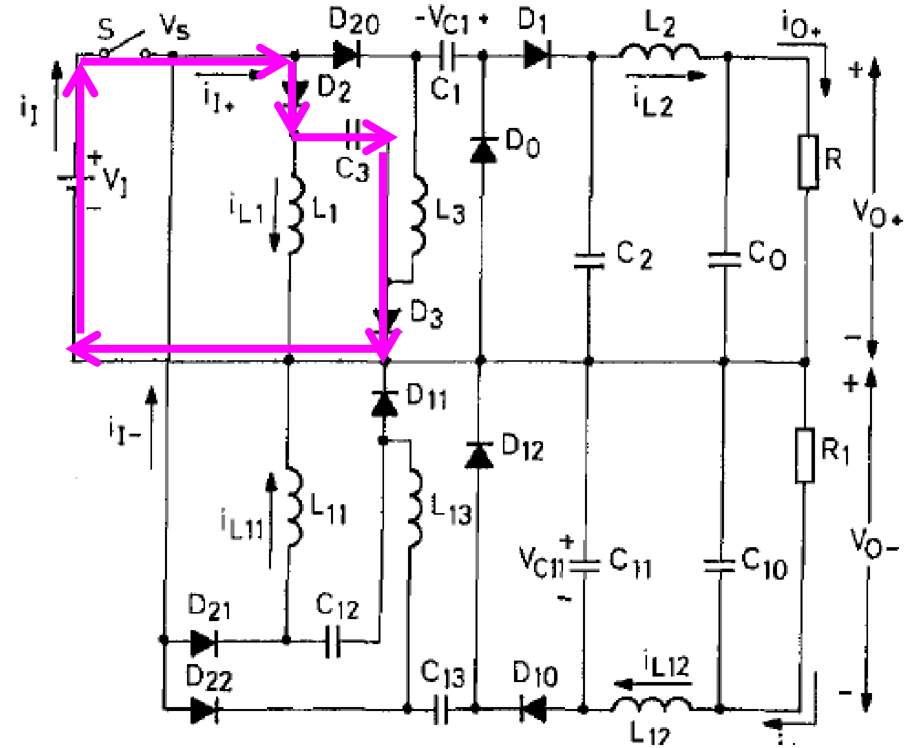
Non-PWM Converters



(a) Two Lift



(b) KY Converter (Non-PWM Converter)



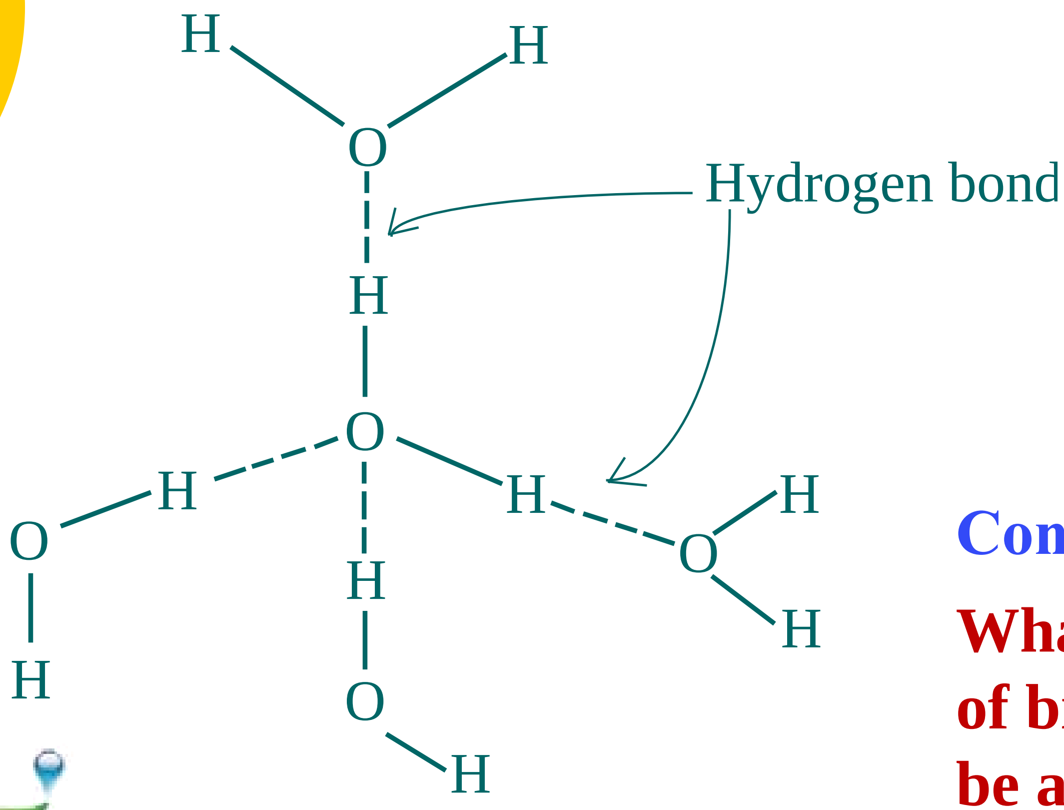
(c) Re-Lift Circuit

Fig. 13.

How to Synthesize PWM Converters?

➢ Compound Concept

- H_2O



- CO_2

$$O = C = O$$

Converter → Element

What is the mechanism of binding converters to be a compound converter?

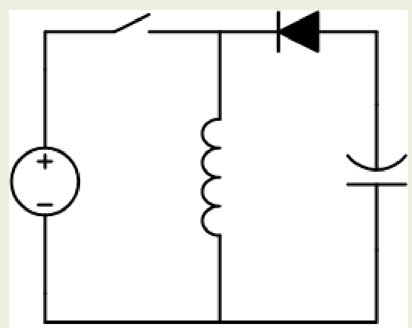
Decoding

A. Approach 1—Component-Interconnection Expression

1) Representing $D \times \frac{1}{1-D}$ in an expression which can inter-connect all components in a certain configuration.

[Buck] ? [Boost] = [Buck-Boost]

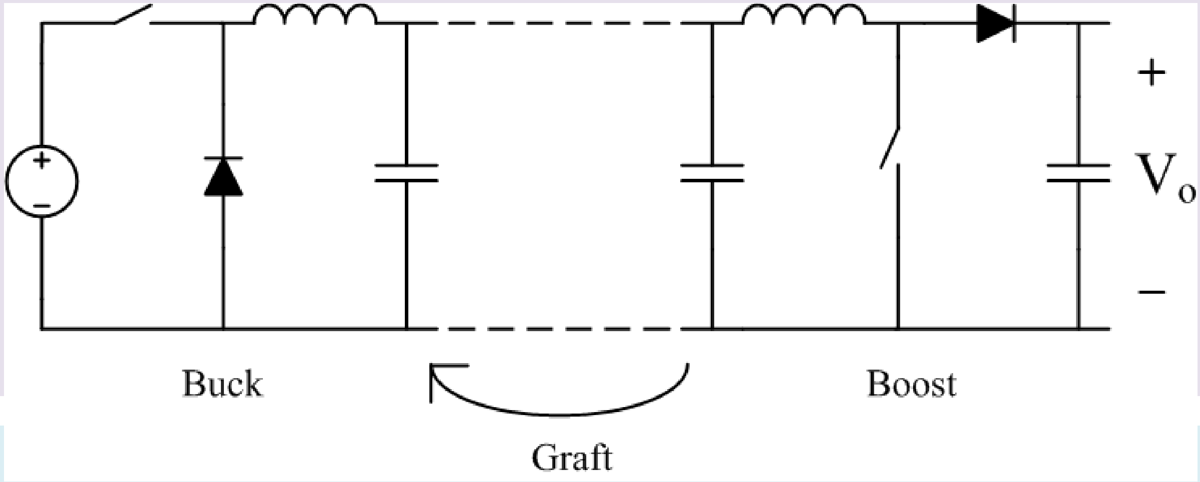
2) Based on the above expression, sketch the final version of the desired converter.



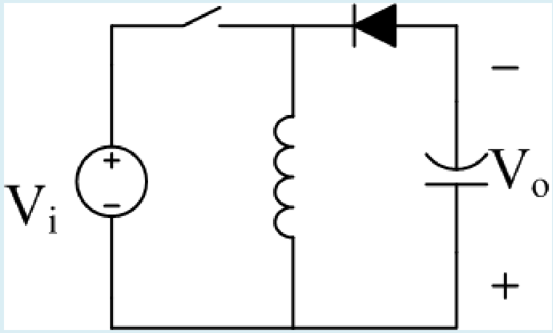
Buck-Boost

2) Approach 2—Transfer-Gain Code Expression

1) Decode $D \times \frac{1}{1-D}$ into two transfer gain codes: *D* and *1/(1-D)* and realize these two codes with two converters.



2) How to synthesize the two converters to become a single one?



Two questions to ask:

1. How to select effective codes?

2. Is there existing an original converter?

II. Input-Output Transfer Curves (Codes)

➢ **Step-Down**

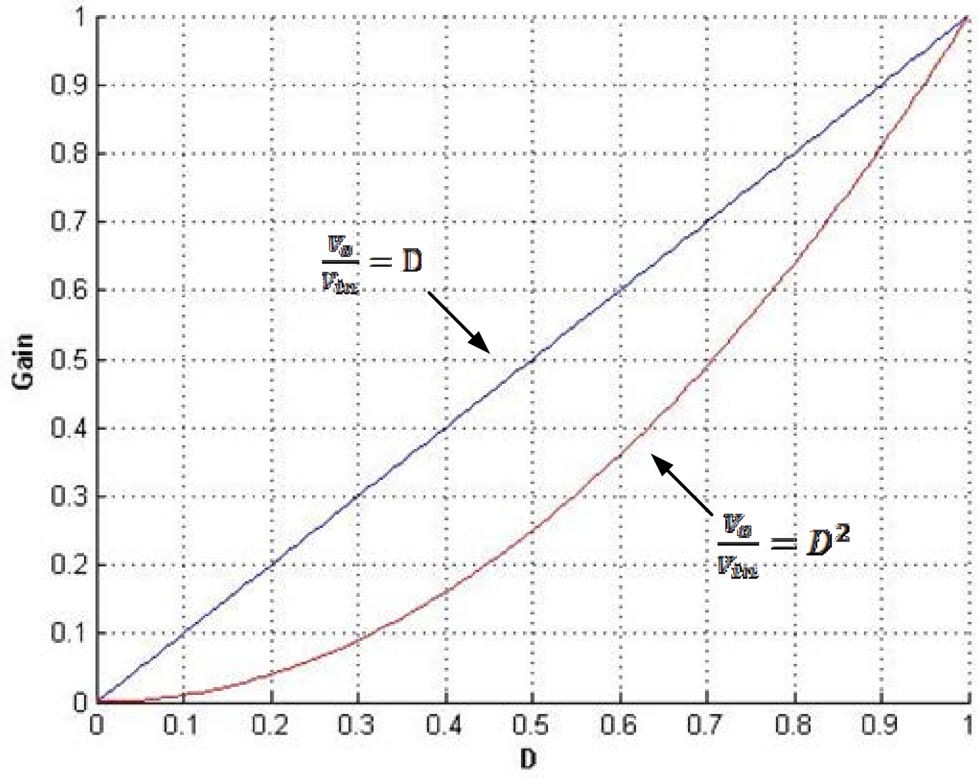


Fig. 1.

➢ Step-Up

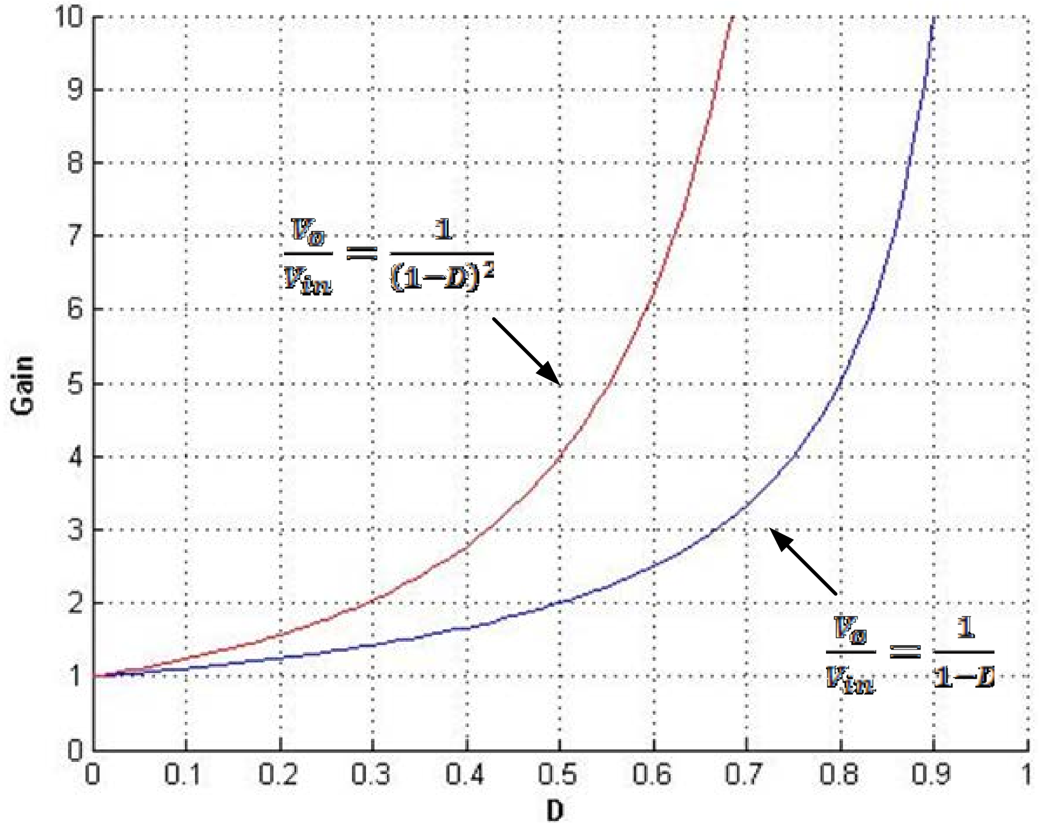

10
9
8
7
6
5
4
3
2
1
0
Gain
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
D
$\frac{V_o}{V_{in}} = \frac{1}{(1-D)^2}$
$\frac{V_o}{V_{in}} = \frac{1}{1-D}$

Fig. 2.

➢ Step-Up and Step-Down

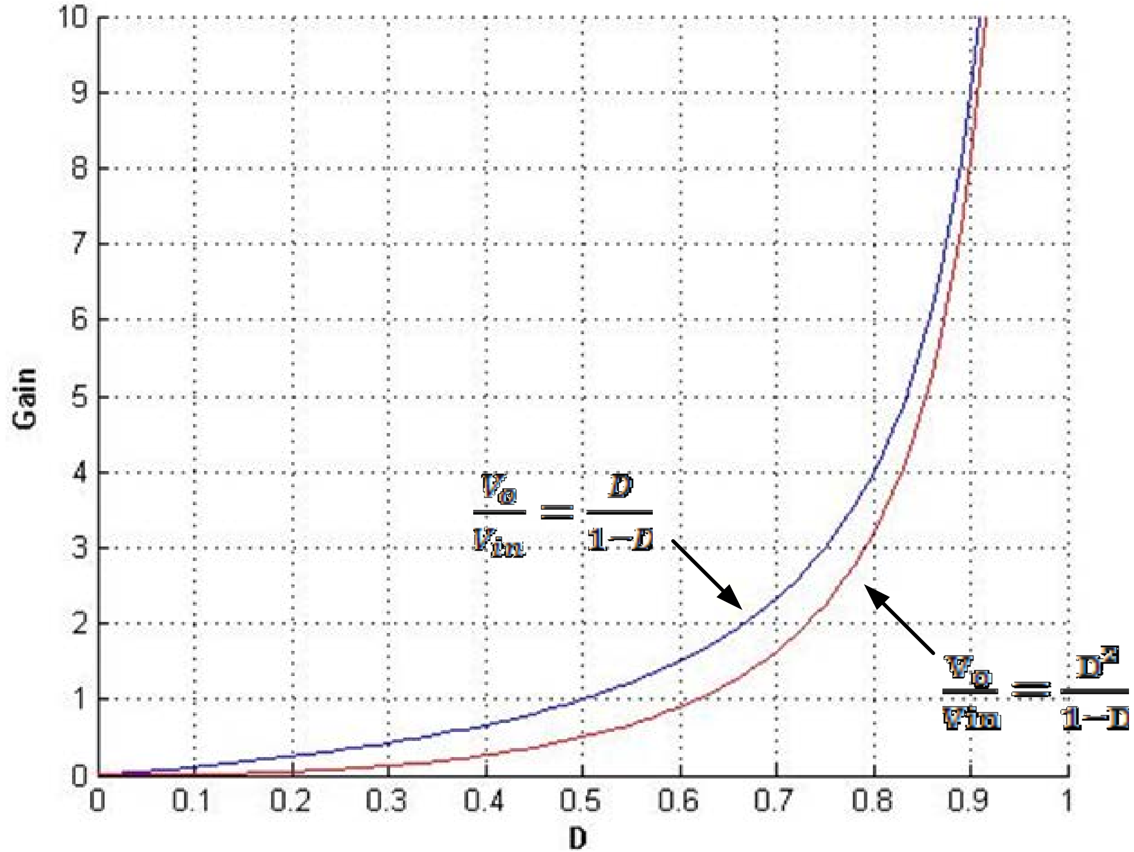


Fig. 3.

± Step-Up and Step-Down

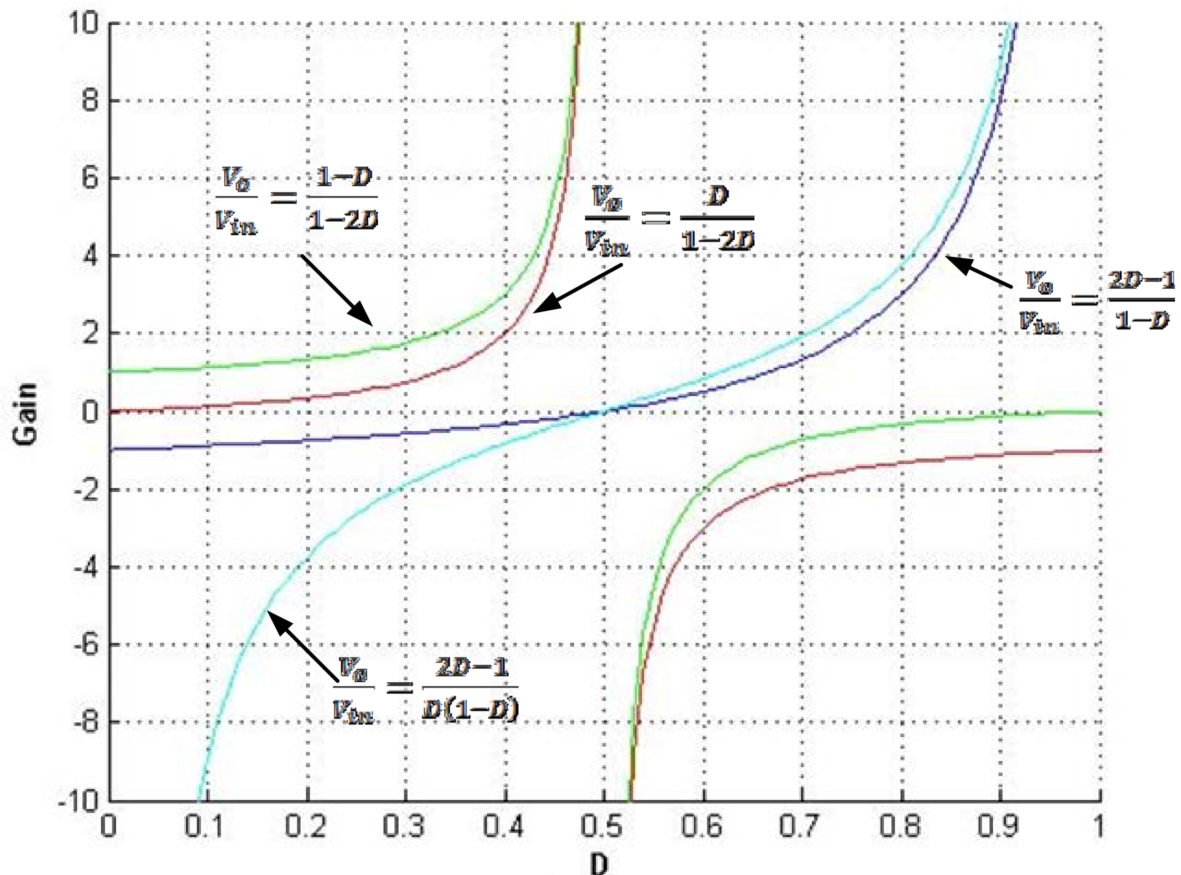


Fig. 4.

III. Origin of Converters

➢ Source-Load Approach

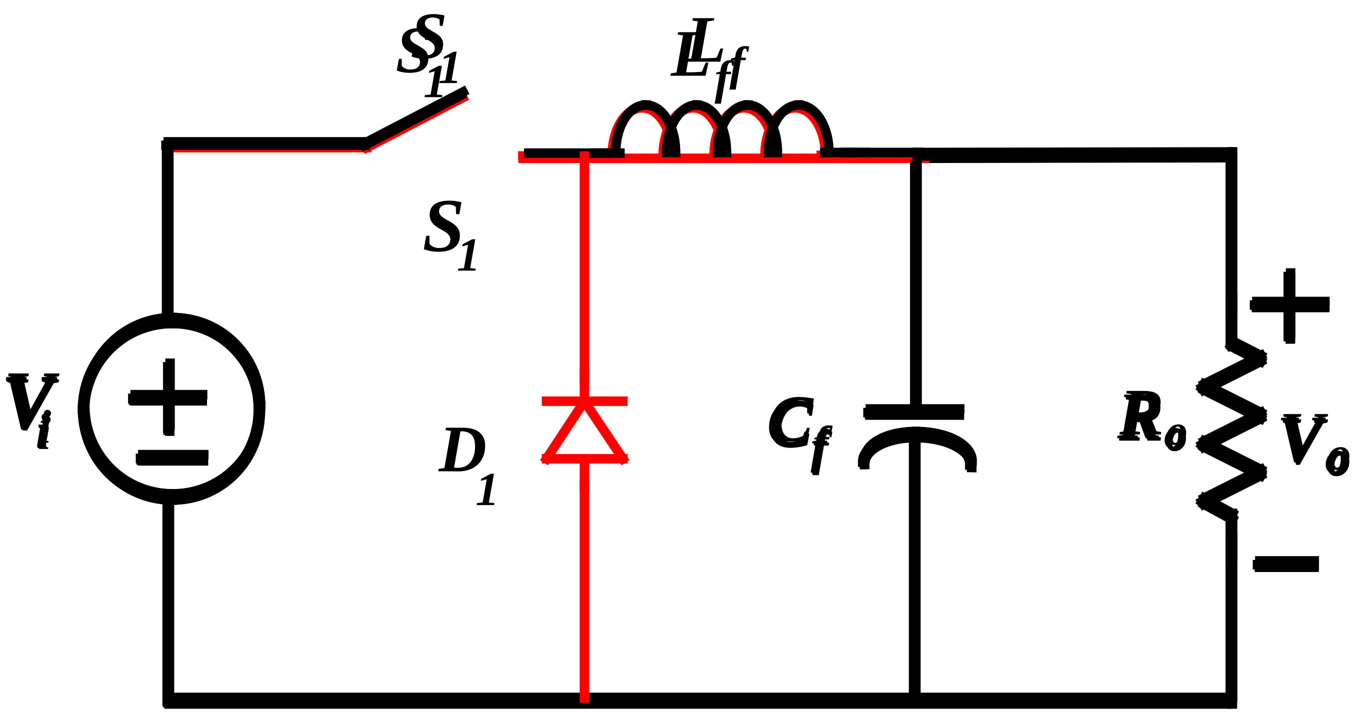
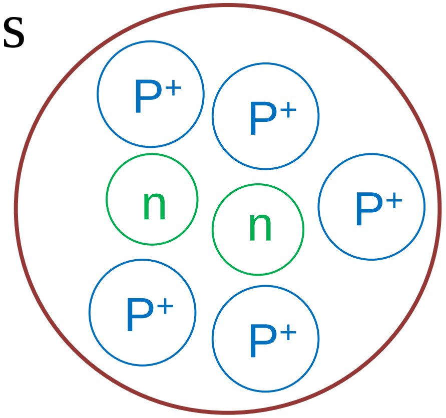


Fig. 1.

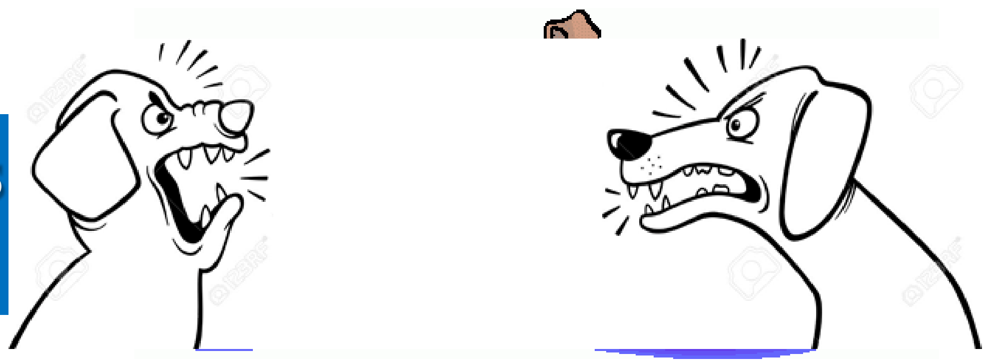
Proton-Meson Approach

Hideki Yukawa

- Awarded the 1949 Nobel Prize in Physics



Protons are dogs and Neutrons are rawhide knotted bones.



Meson is the carrier of the nuclear force that holds nuclei together.

- Buck Converter

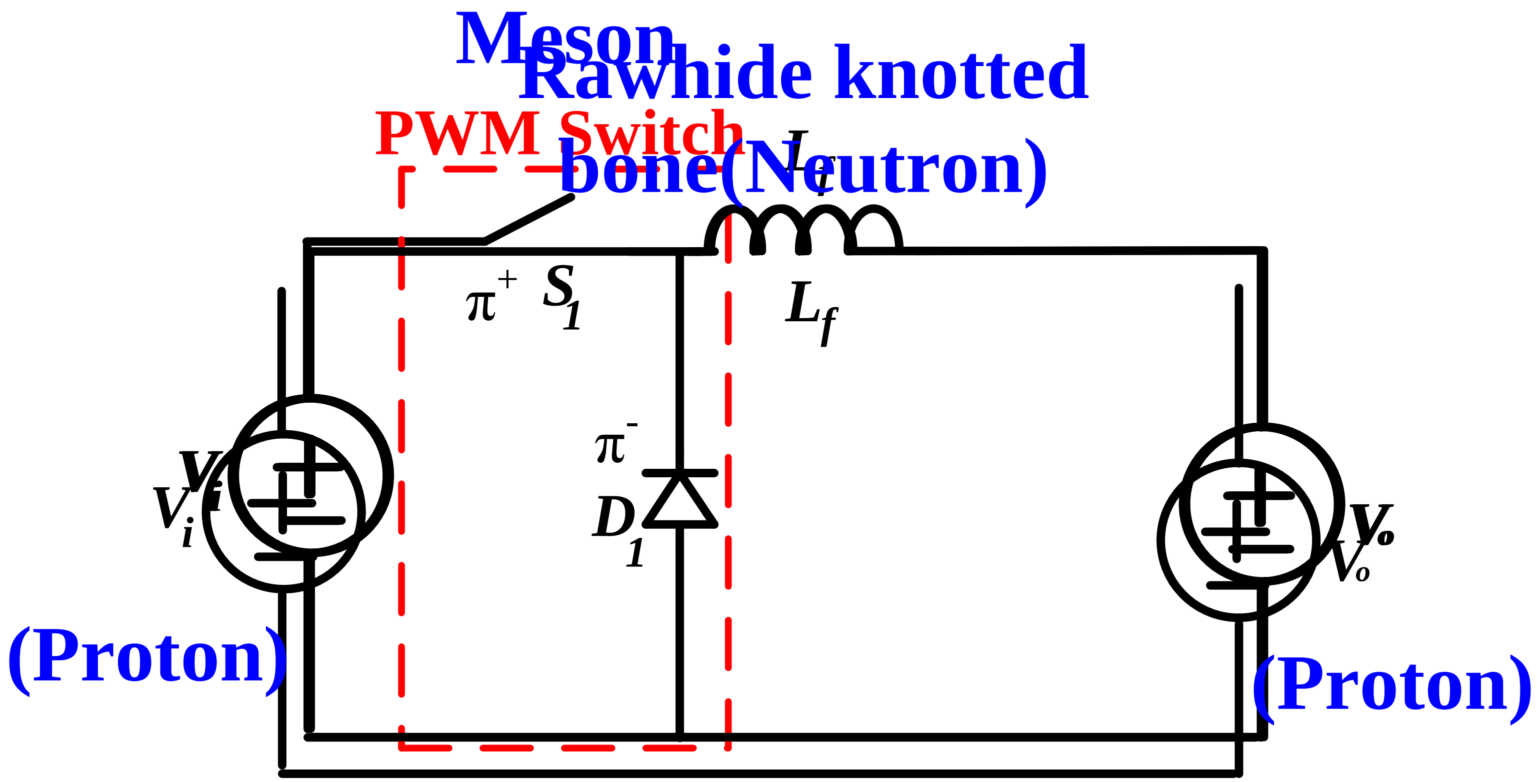


Fig. 2.

Resonance Approach

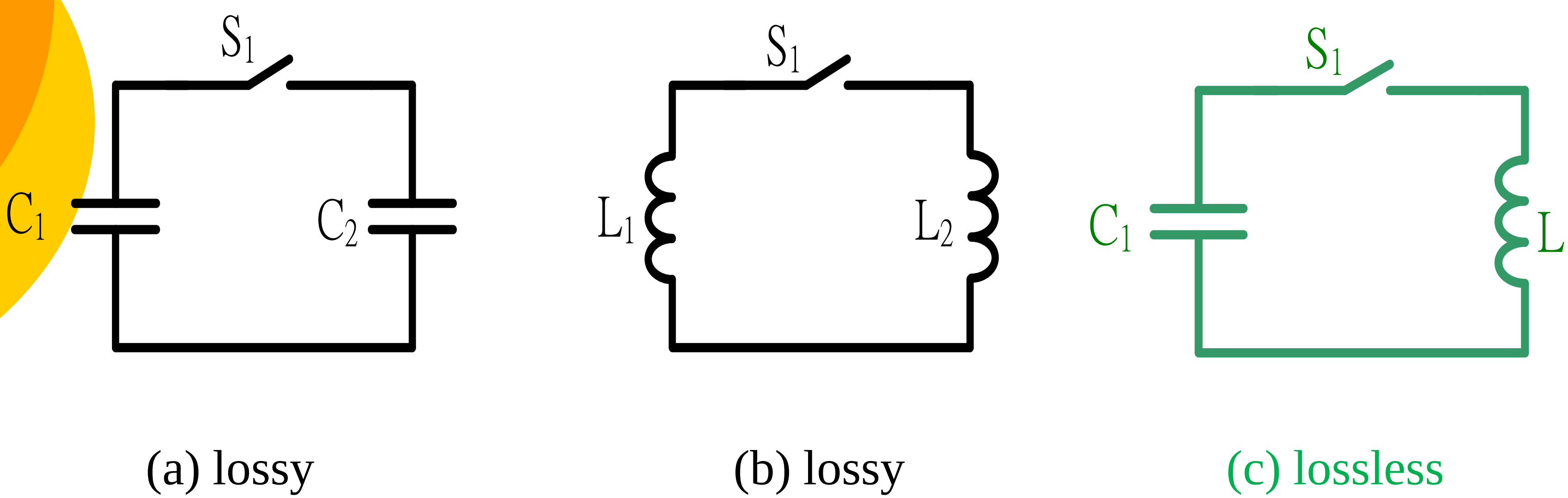


Fig. 3. Three types of configurations of power transfer between capacitor and inductor.

➢ The Original Converter

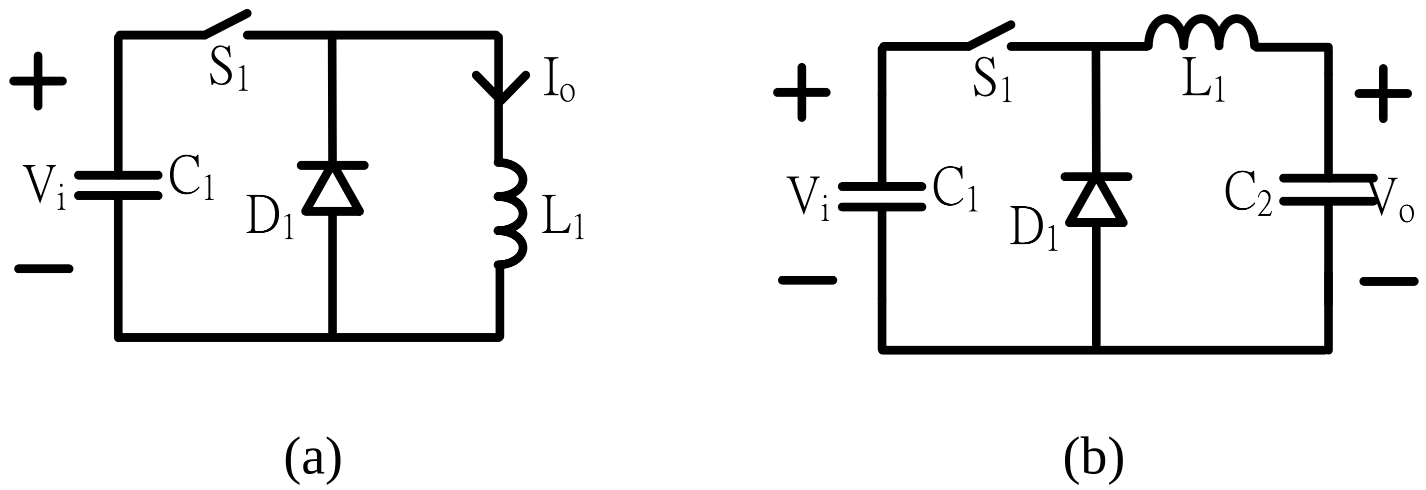


Fig. 4. A practical example applying the resonance concept.

IV. Graft Scheme

➢ Conventional Approaches to Deriving Converters

- P cell and N cell [20]

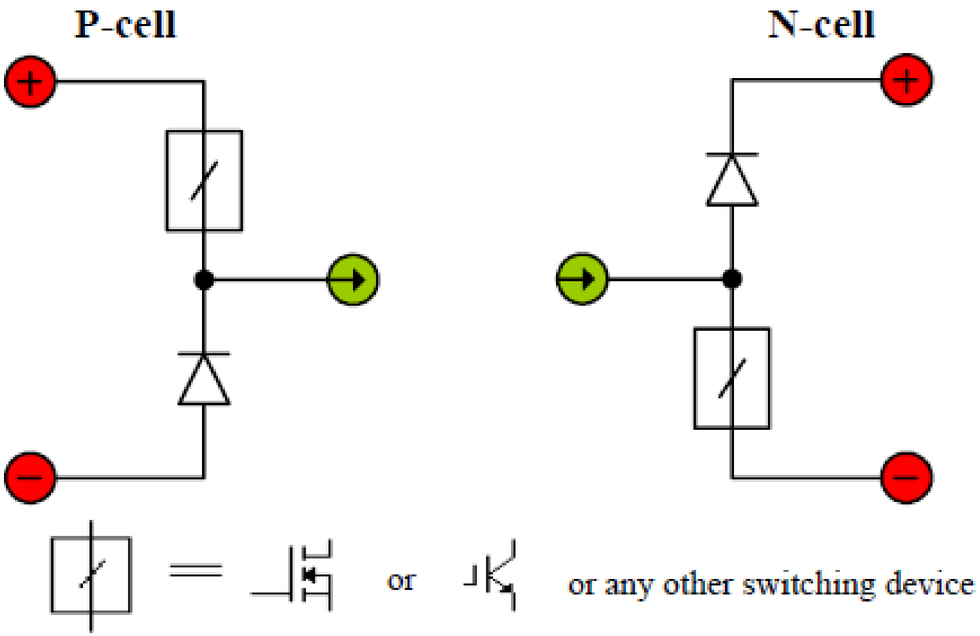


Fig. 1. Two basic switching cells: P-cell and N-cell. Terminal (+) connects to the positive lead of a voltage-source or capacitor, (−) connects to the negative lead of a voltage-source or capacitor, (→) connects to the positive lead of a current-source or inductor, and (←) connects to the negative lead of a current-source or inductor. The switching device can be a MOSFET, IGBT, or other controlled semiconductor switching device.

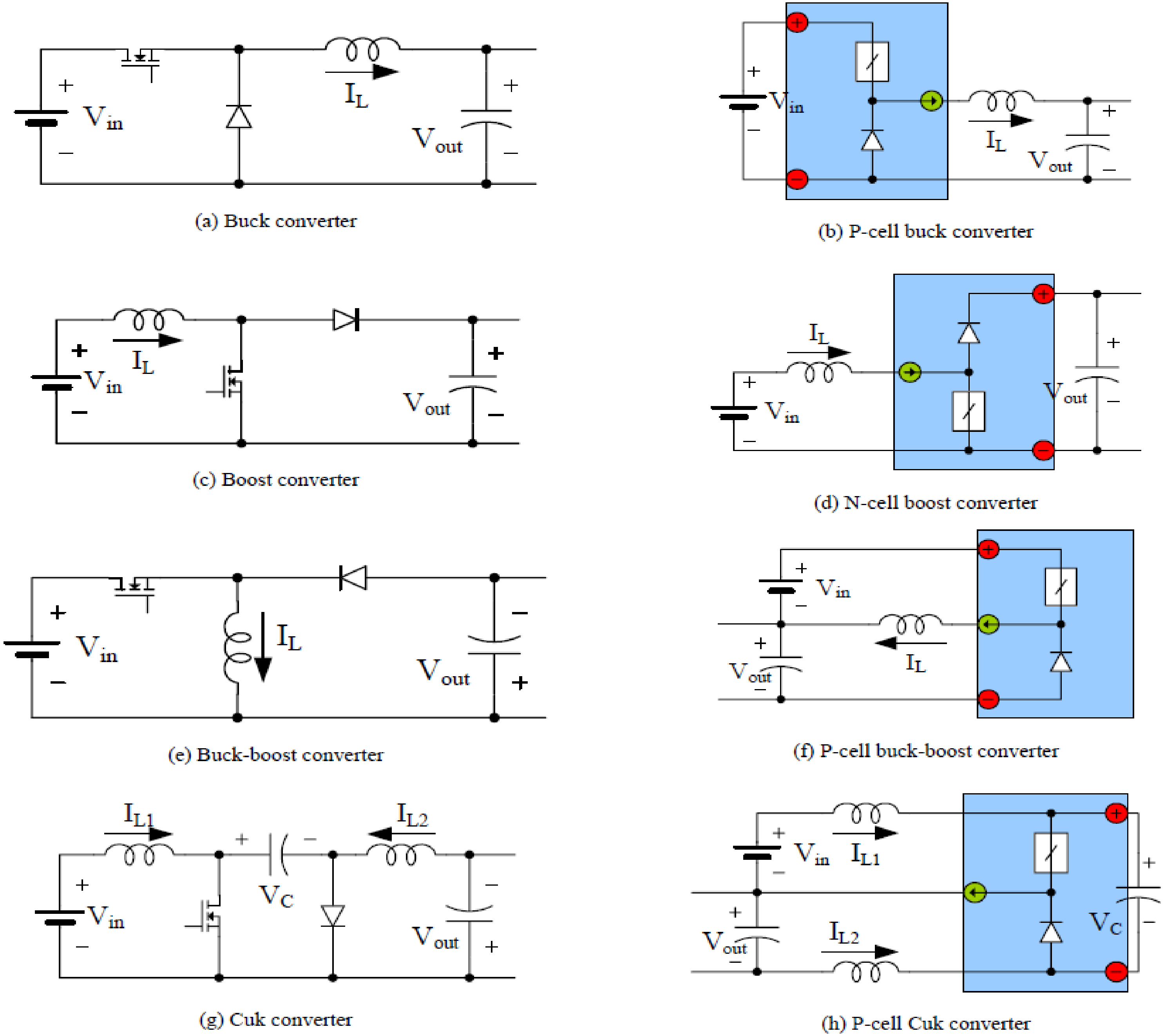


Fig. 2. The dc-dc converters and their construction by the basic cells.

• Canonical Switching Cells [24], [29]

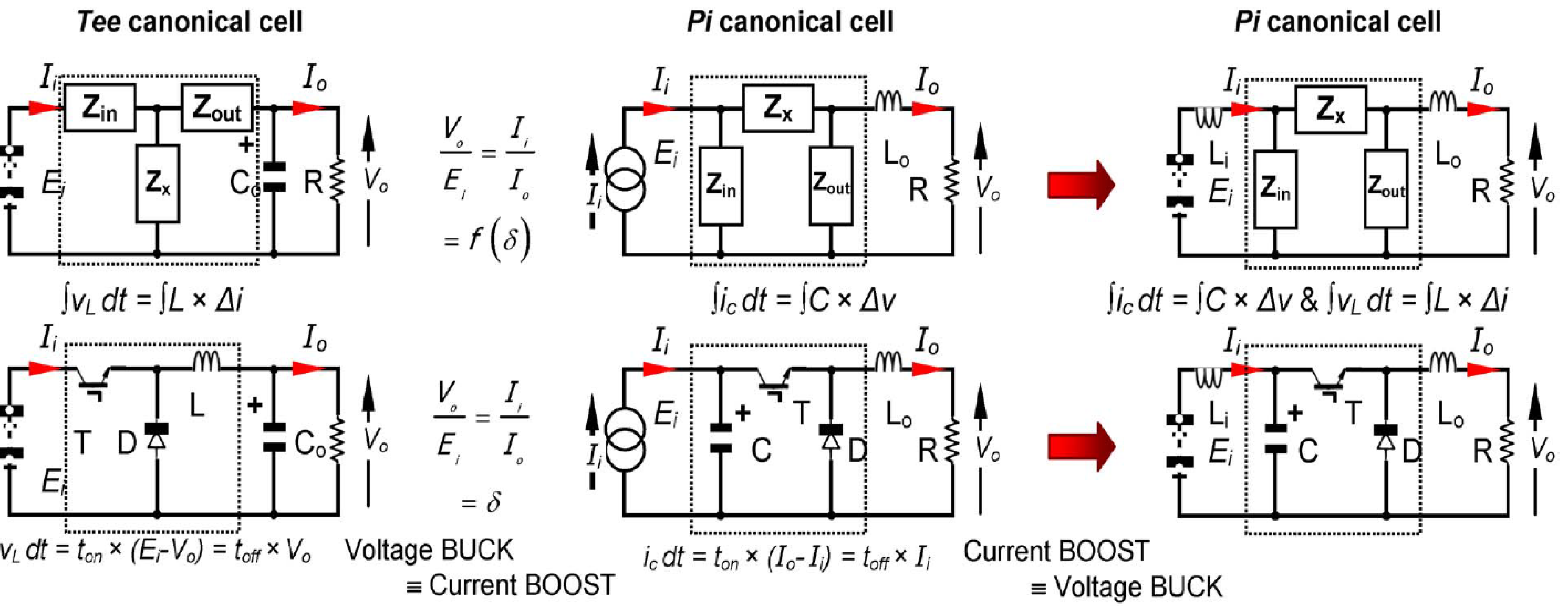


Fig. 3.

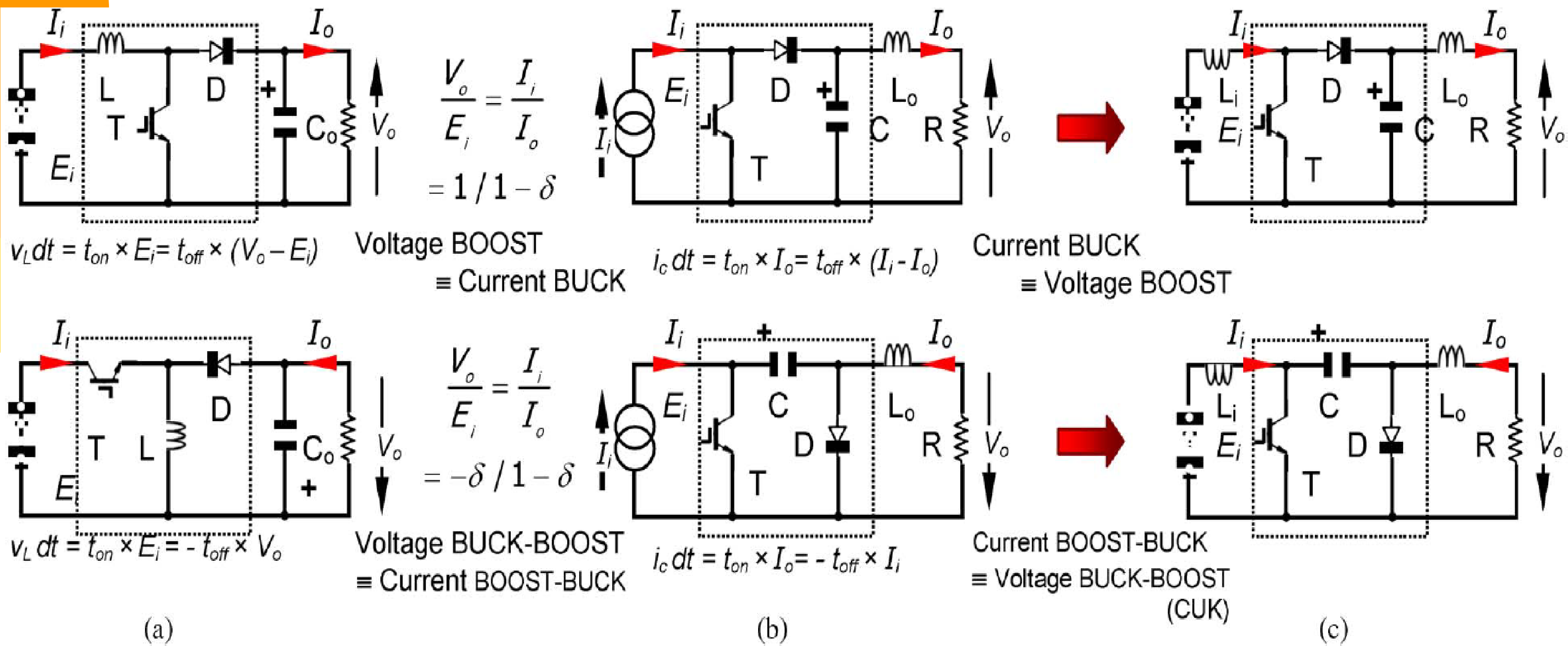

$v_L dt = t_{on} \times E_i = t_{off} \times (V_o - E_i)$
$\frac{V_o}{E_i} = \frac{I_i}{I_o} = 1/1-\delta$
Voltage BOOST
≡ Current BUCK
$i_c dt = t_{on} \times I_o = t_{off} \times (I_i - I_o)$
Current BUCK
≡ Voltage BOOST
$v_L dt = t_{on} \times E_i = - t_{off} \times V_o$
$\frac{V_o}{E_i} = \frac{I_i}{I_o} = -\delta/1-\delta$
Voltage BUCK-BOOST
≡ Current BOOST-BUCK
$i_c dt = t_{on} \times I_o = - t_{off} \times I_i$
Current BOOST-BUCK
≡ Voltage BUCK-BOOST
(CUK)
(a)
(b)
(c)

Fig. 4.

- Switched-Cap./Ind. Cells [48]

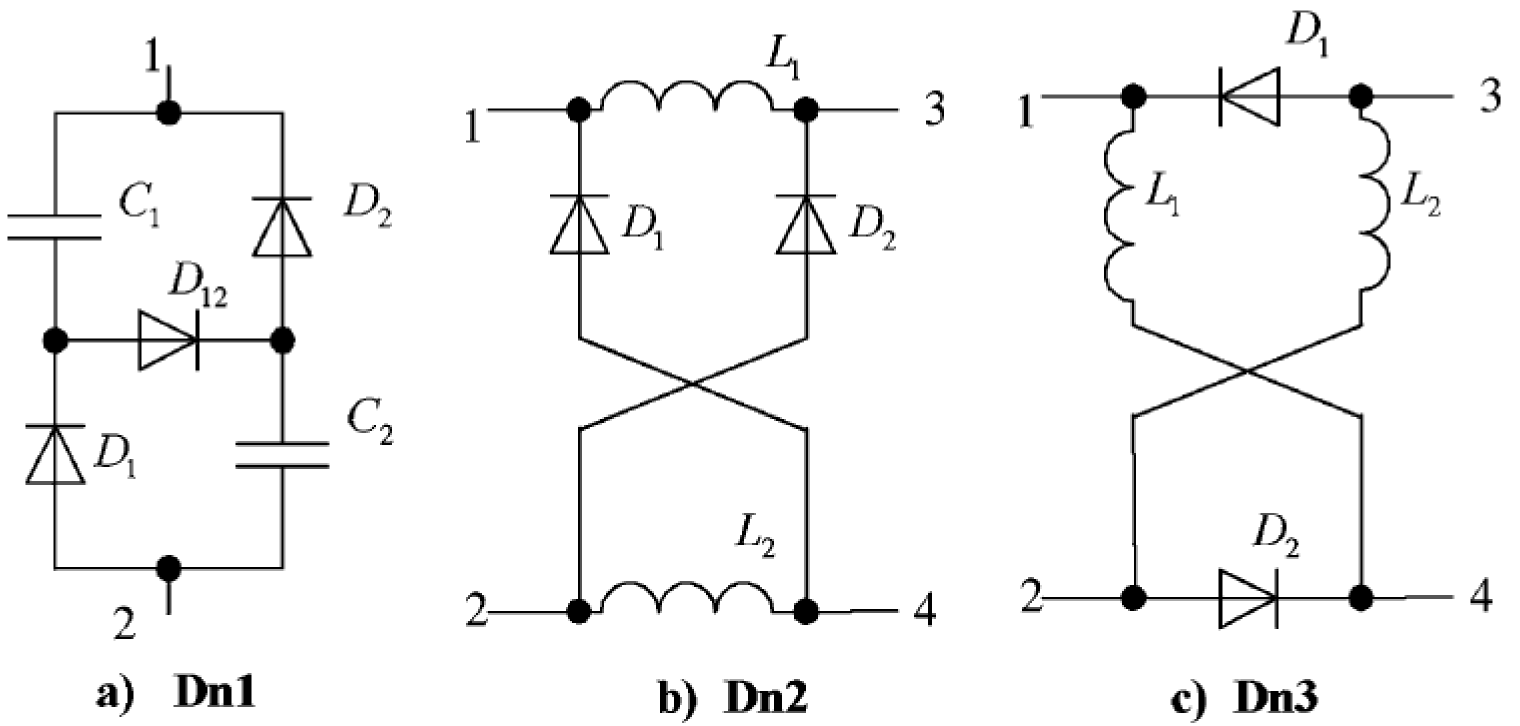


Fig. 5. Step-down basic switching structures.

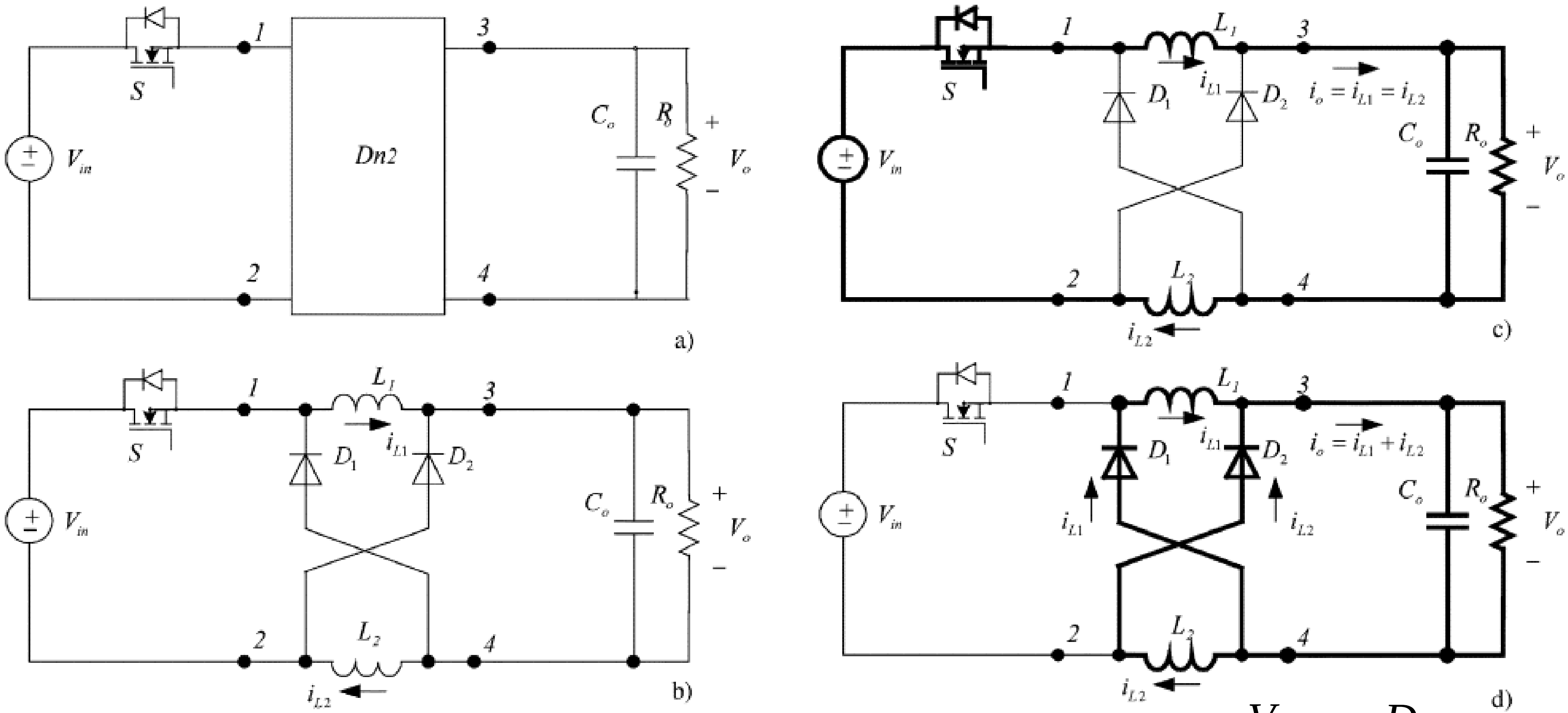
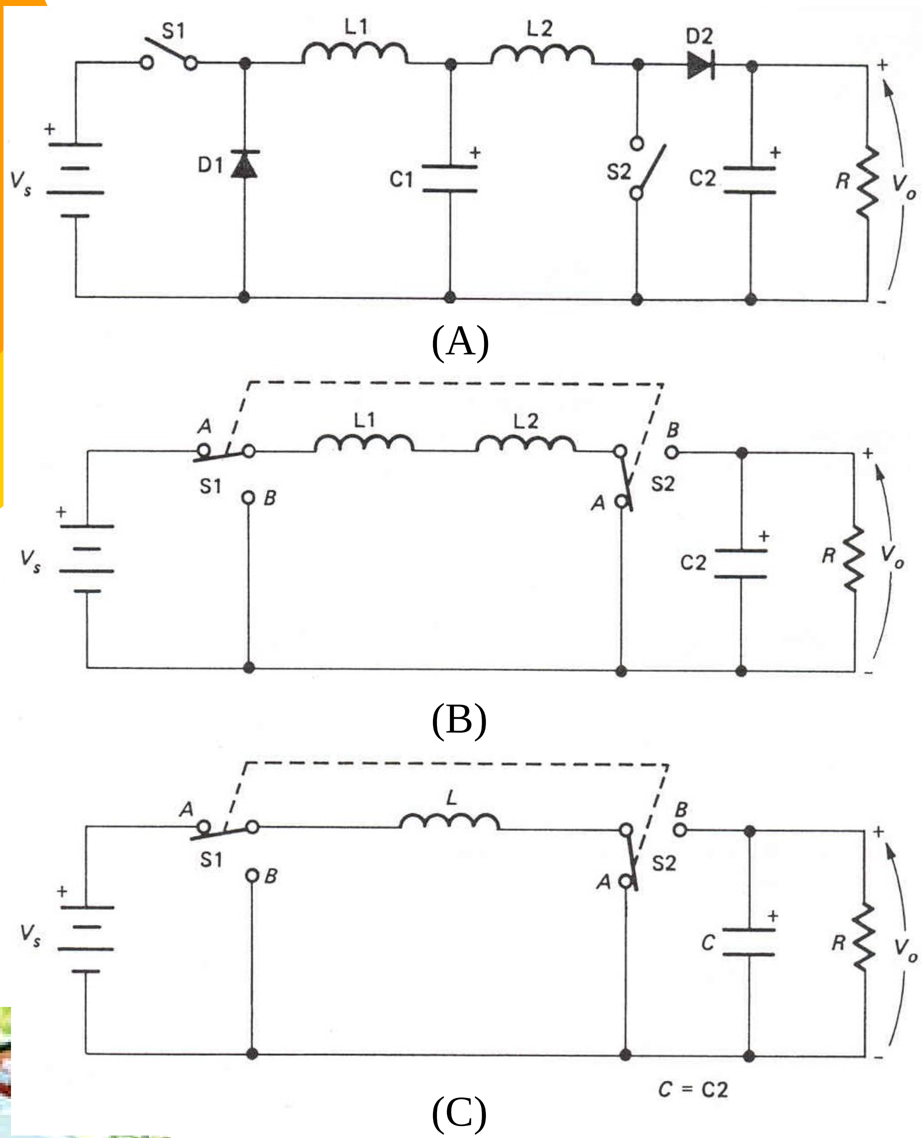


Fig. 6.

$$\frac{V_O}{V_{in}} = \frac{D}{2-D}$$

• Synchronous Switches [3]



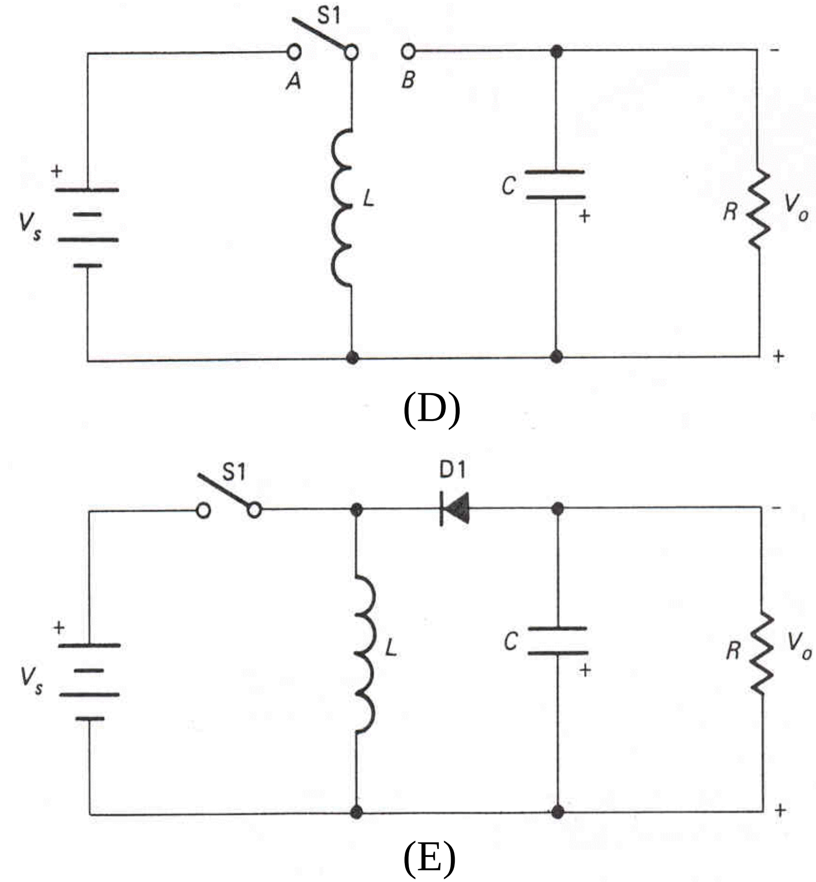


Fig. 7. Evolution of the buck-boost converter

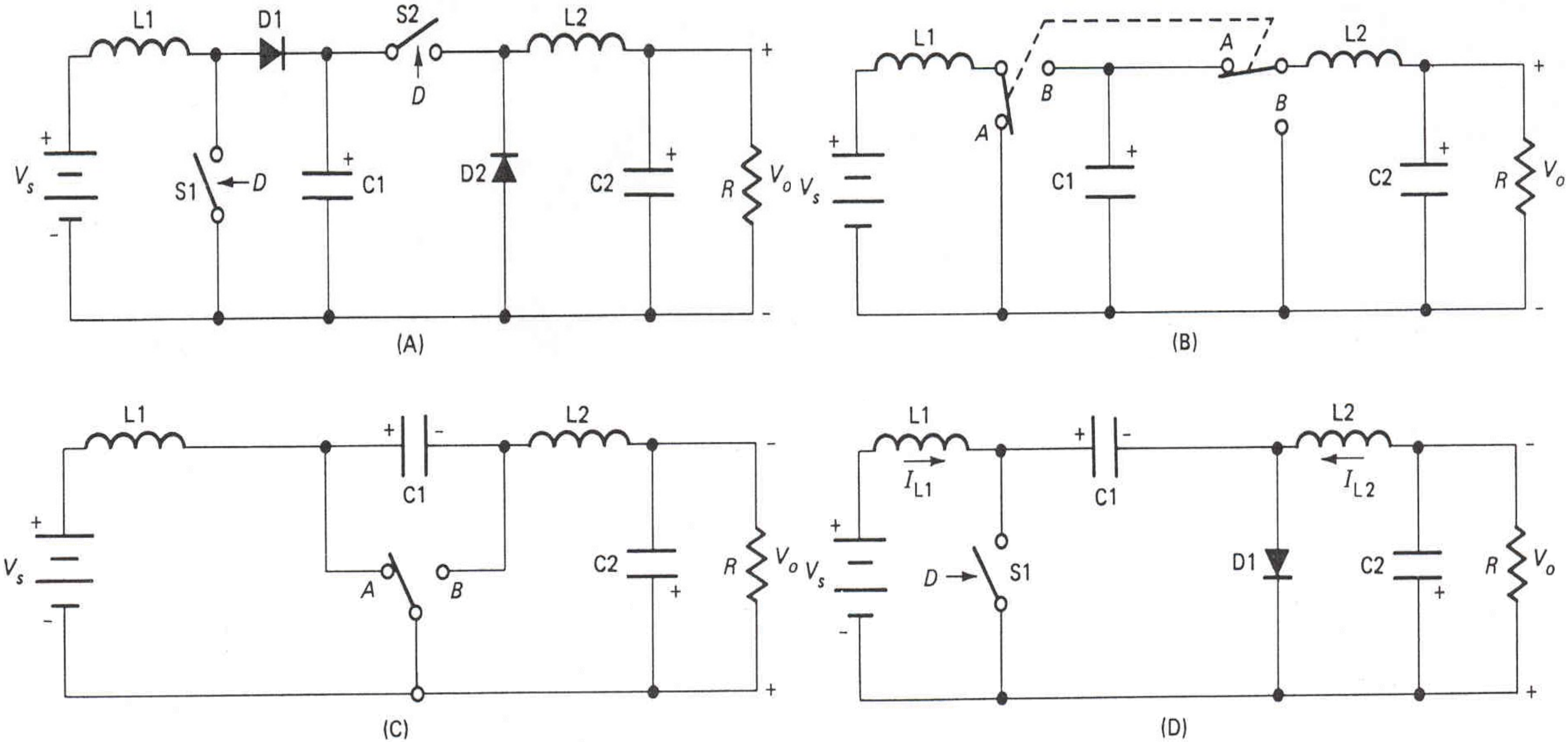


Fig. 8. Evolution of the Ćuk converter.

➢ with Grafted Switches

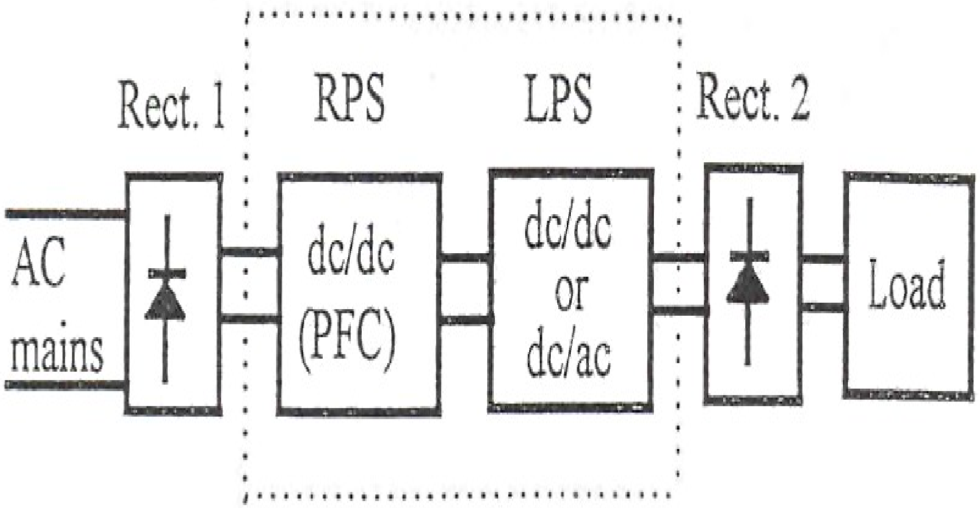


Fig. 9.

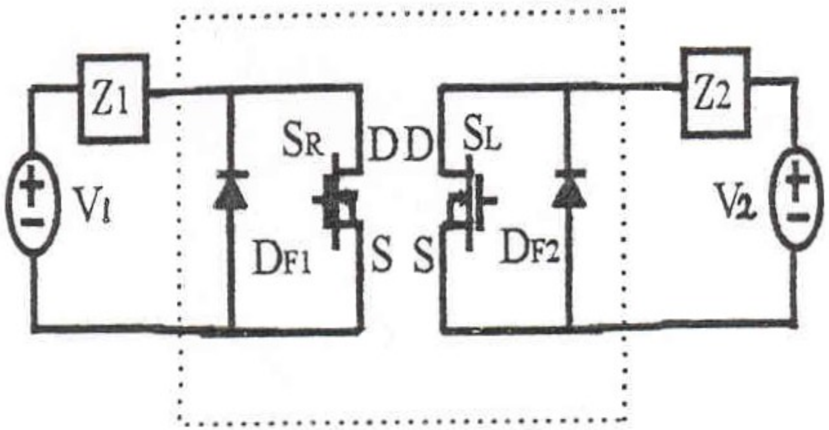


Fig. 10.

• T-type Grafted Switches

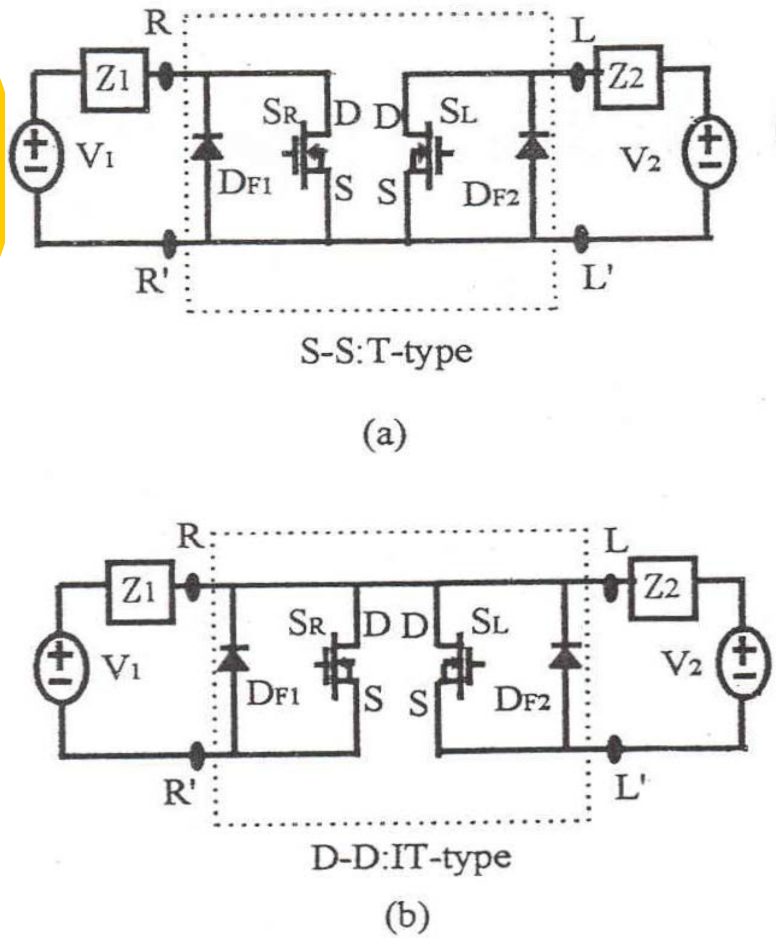


Fig. 11.

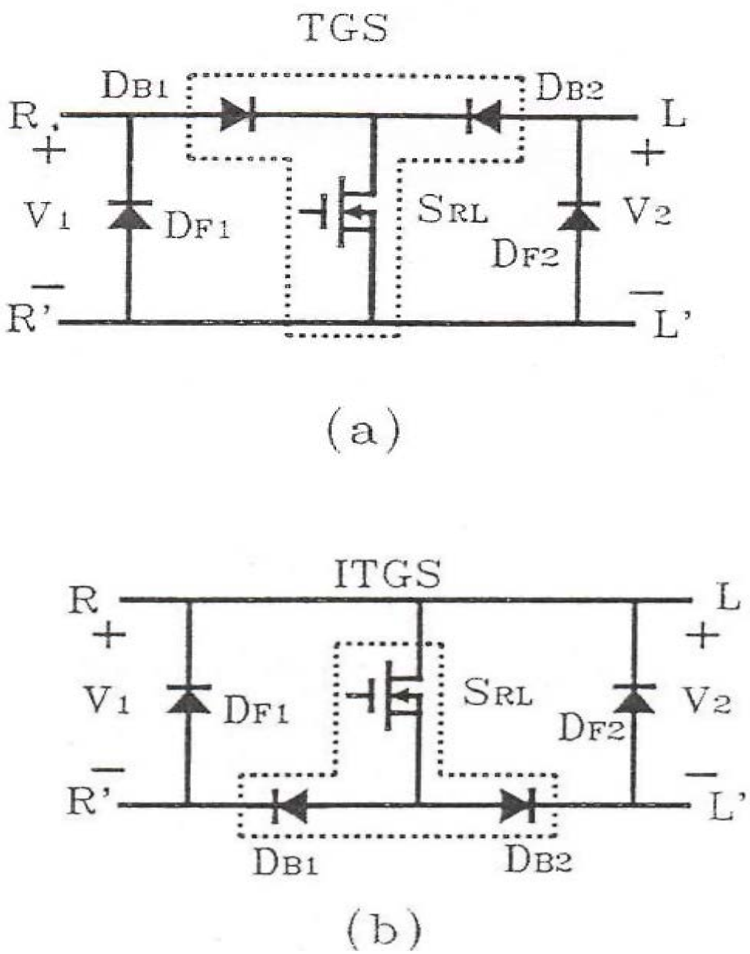
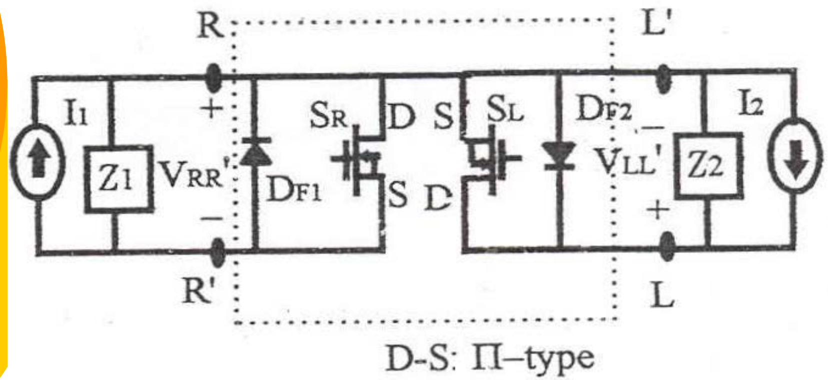
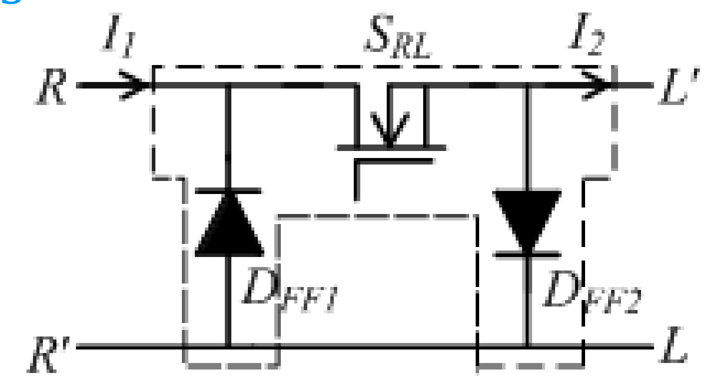


Fig. 12.

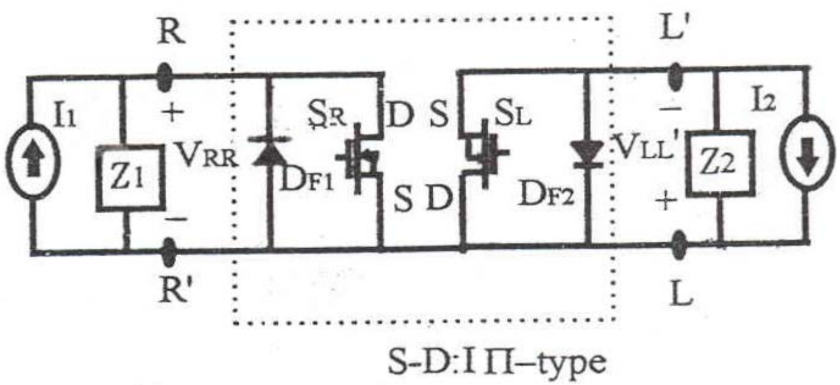
- π-type Grafted Switches



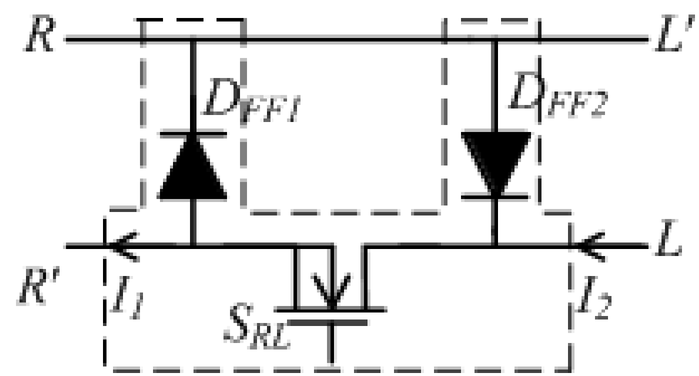
(c)



(c)



(d)



(d)

Fig. 13.

Fig. 14.

Table 1

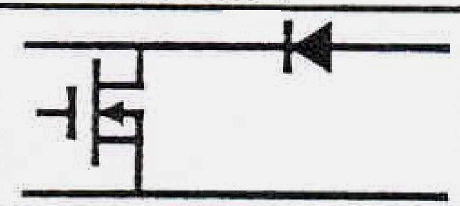
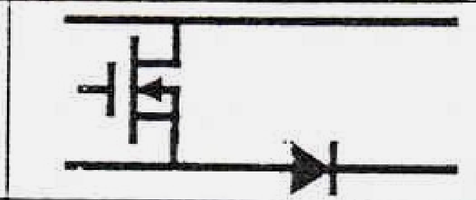
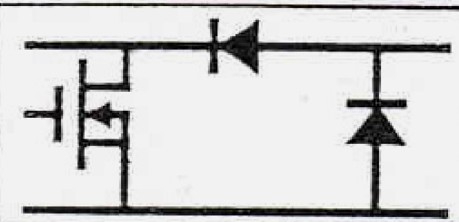
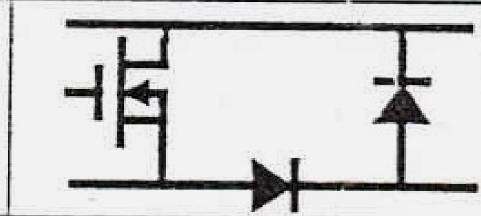
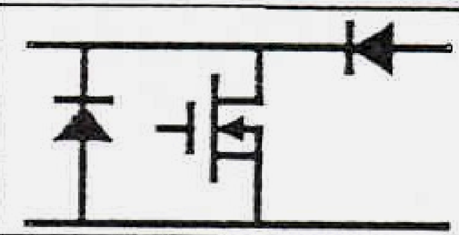
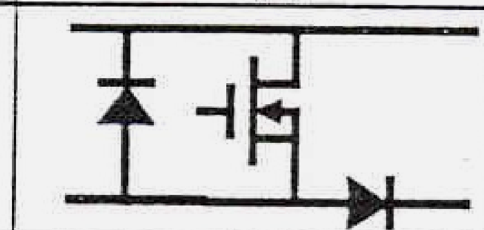
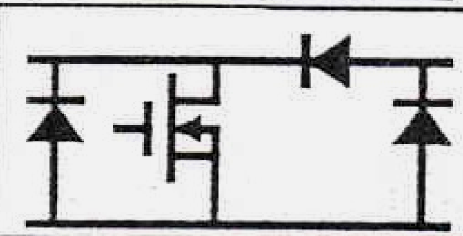
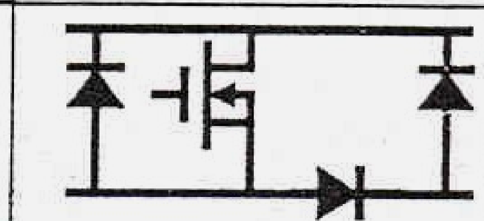
Relationship between voltage sources	Original Switches		Degenerated T-type Grafted Switch (DTGS)	Degenerated Inverted T-type Grafted Switch (DITGS)
	S1	S2		
$V_1 > V_2$	U	U		
	U	B		
	B	U		
	B	B		

Table 2

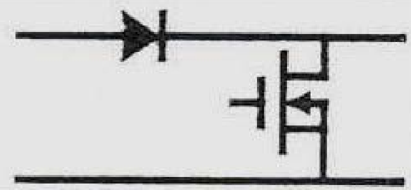
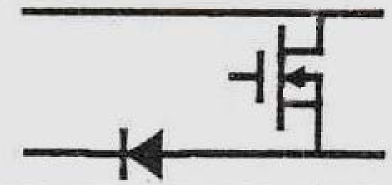
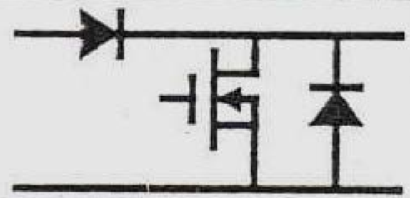
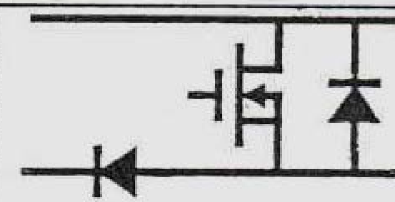
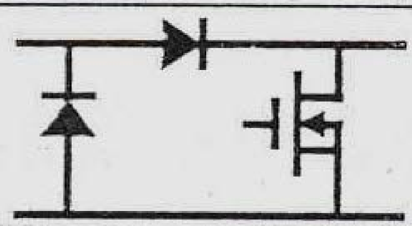
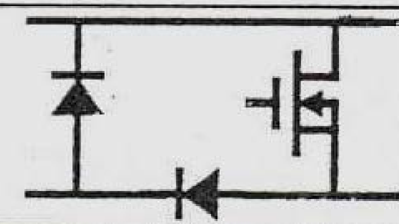
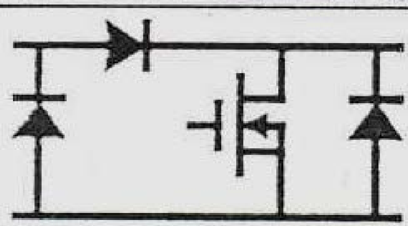
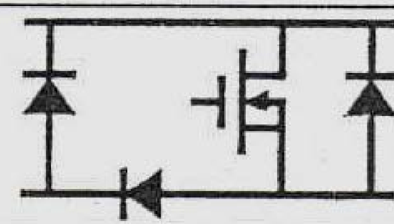
Relationship between voltage sources	Original Switches		Degenerated T-type Grafted Switch (DTGS)	Degenerated Inverted T-type Grafted Switch (DITGS)
	S1	S2		
$V_1 < V_2$	U	U		
	U	B		
	B	U		
	B	B		

Table 3

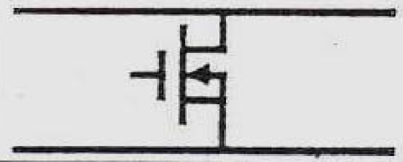
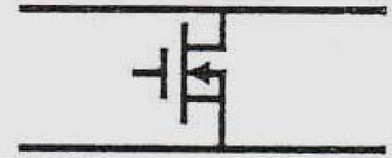
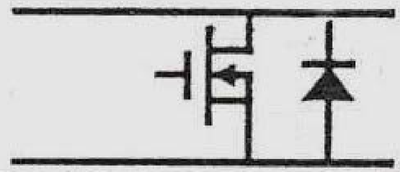
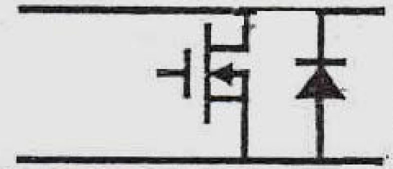
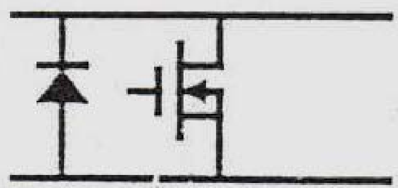
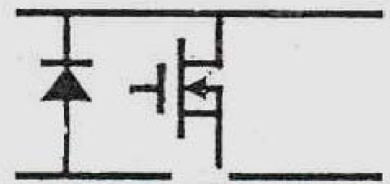
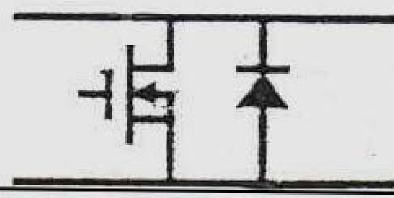
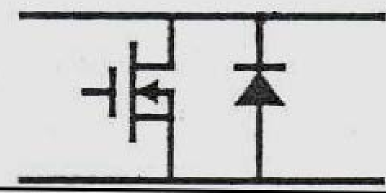
Relationship between voltage sources	Original Switches		Degenerated T-type Grafted Switch (DTGS)	Degenerated Inverted T-type Grafted Switch (DITGS)
	S1	S2		
$V_1 = V_2$	U	U		
	U	B		
	B	U		
	B	B		

Table 4

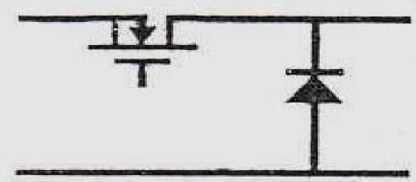
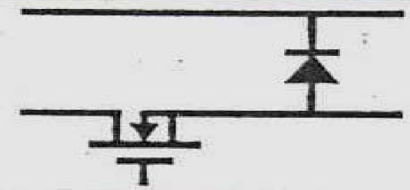
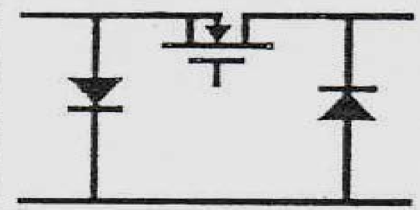
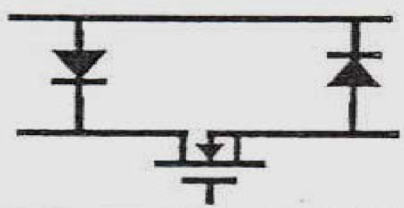
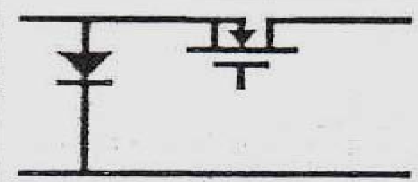
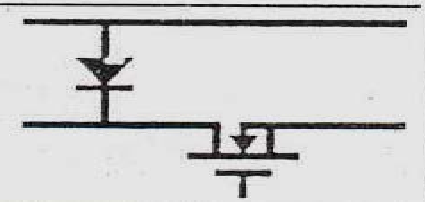
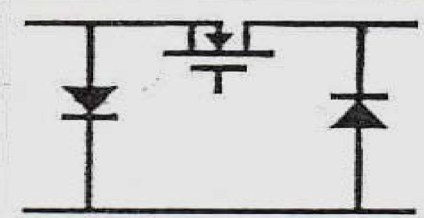
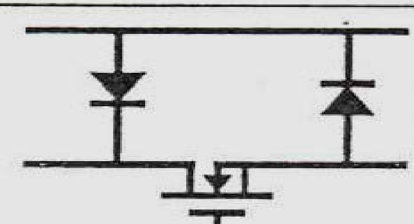
Relationship between current sources	Original Switches S1	Original Switches S2	Degenerated Π-type Grafted Switch (DΠGS)	Degenerated Inverted Π-type Grafted Switch (DIΠGS)
$I_1 > I_2$	U	U		
	U	B		
	B	U		
	B	B		
$I_1 < I_2$	U	U		
	B	U		
	U	B		
	B	B		

Table 5

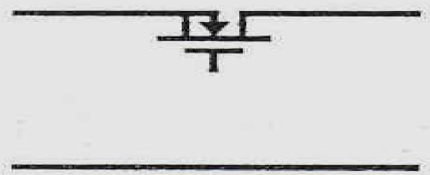
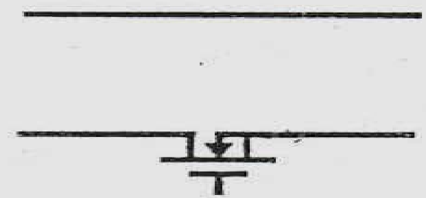
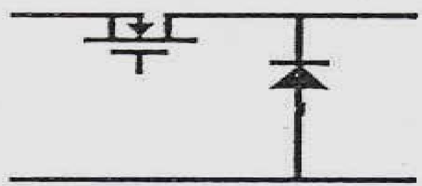
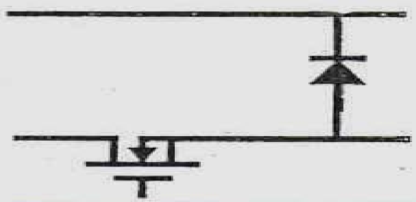
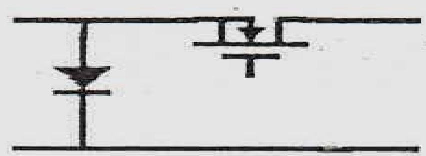
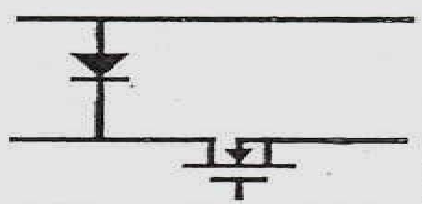
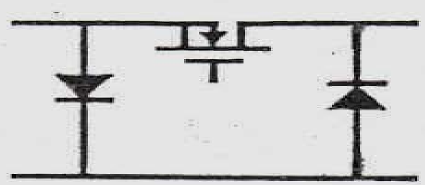
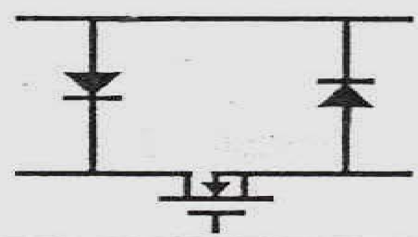
Relationship between current sources	Original Switches		Degenerated Π-type Grafted Switch (DΠGS)	Degenerated Inverted Π-type Grafted Switch (DIΠGS)
	S1	S2		
$I_1 = I_2$	U	U		
	U	B		
	B	U		
	B	B		

Table 6. Duality between T-type and II-type grafted switches

TGS and ITGS	IIGS and IIIGS
1. D_{B1}, D_{B2} and S_{RL} share a node.	1. D_{FF1}, D_{FF2} and S_{RL} form a loop.
2. D_{Bi} blocks the voltage difference between V_1 and V_2 when both switches S_R and S_L are in the off states.	2. D_{FFi} circulates the current difference between I_1 and I_2 when both switches S_R and S_L are in the on states.
3. Required to determine the V_1 and V_2 when S_R and S_L are in the off states.	3. Required to determine the I_1 and I_2 when S_R and S_L are in the on states.
4. Power processors are represented by TECs.	4. Power processors are represented by NECs.

Illustration of Buck-Boost Integration

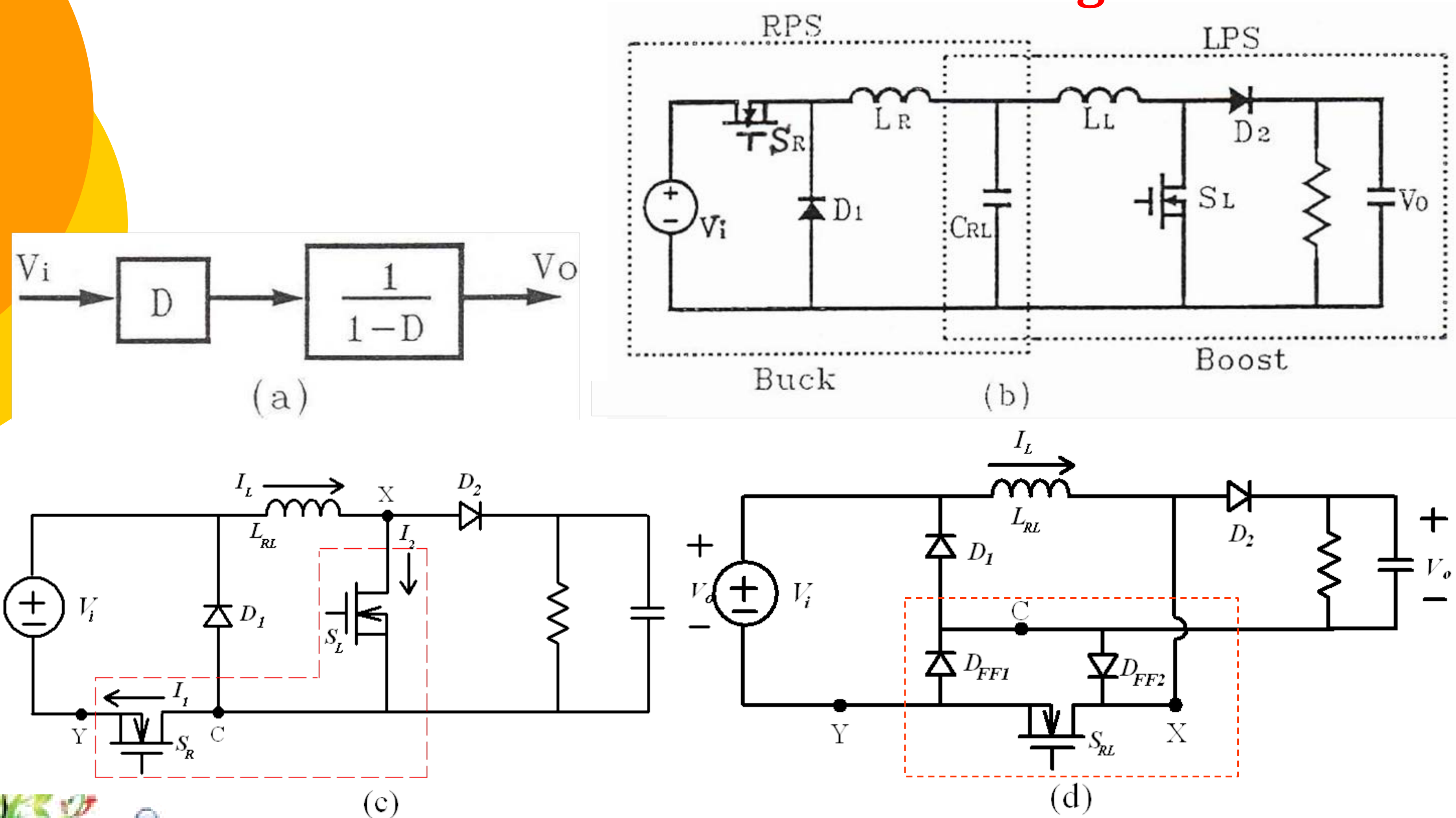


Fig. 15.

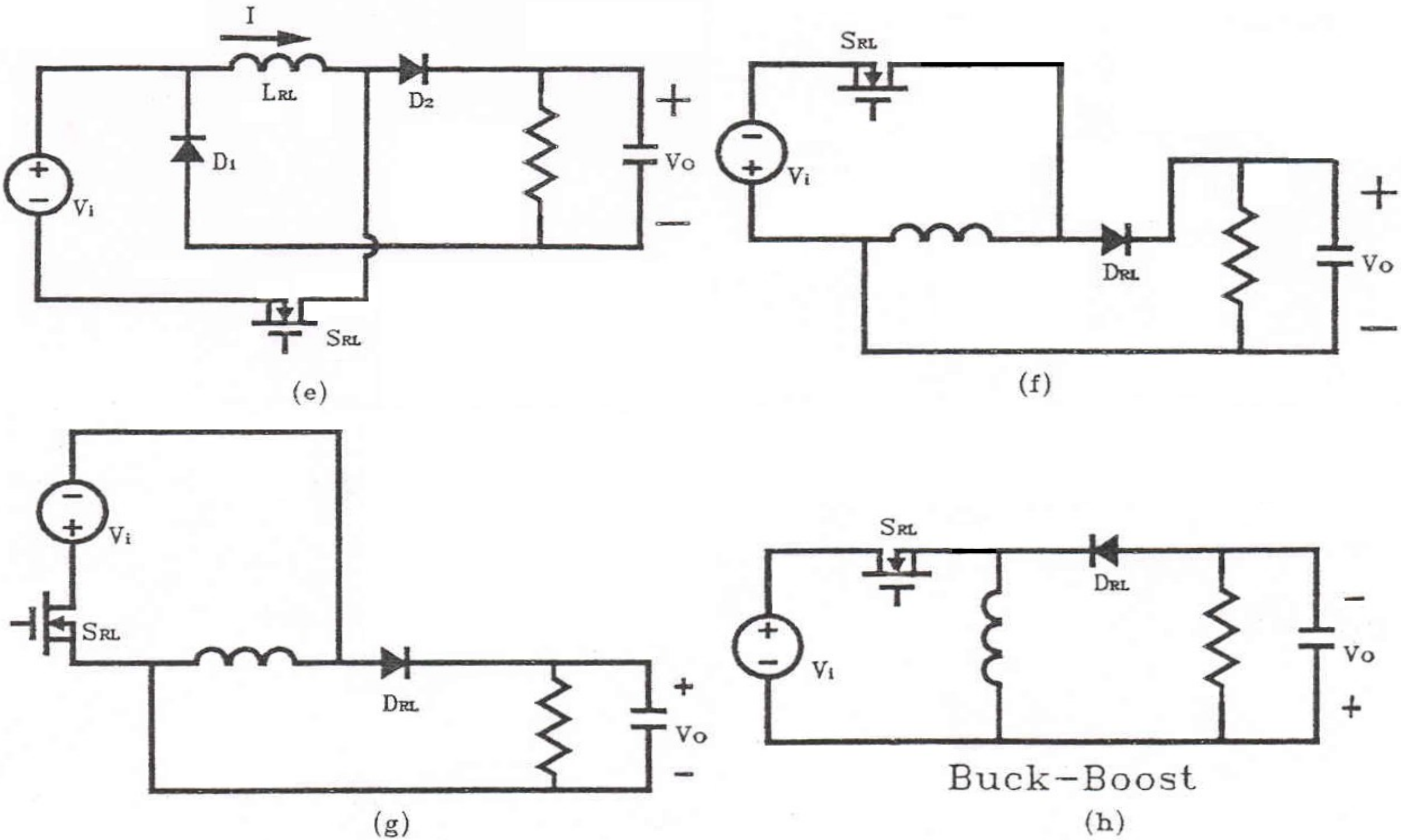


Fig. 15. (continued)

Illustration of Boost-Buck (Ćuk) Integration

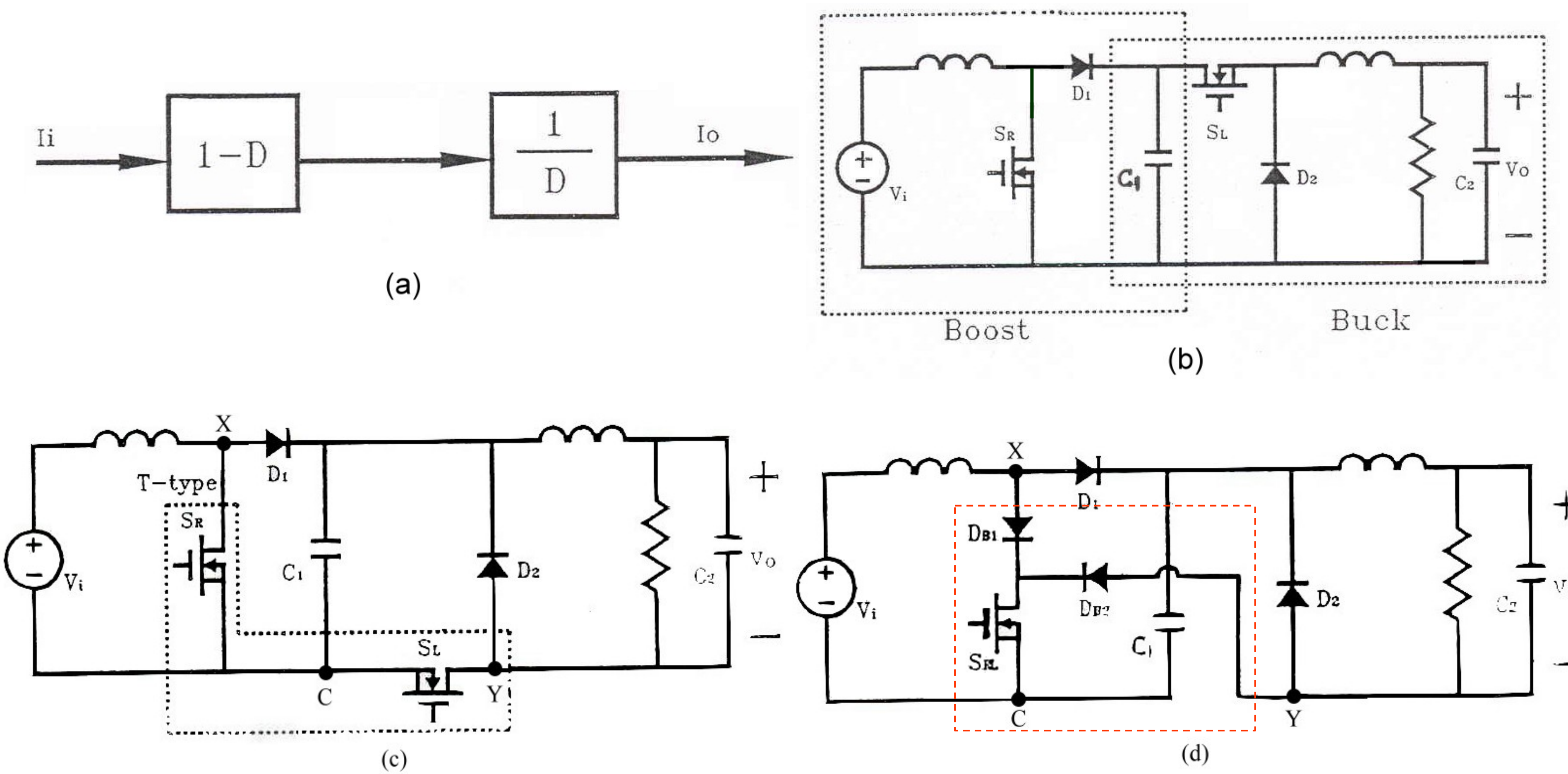


Fig. 16.

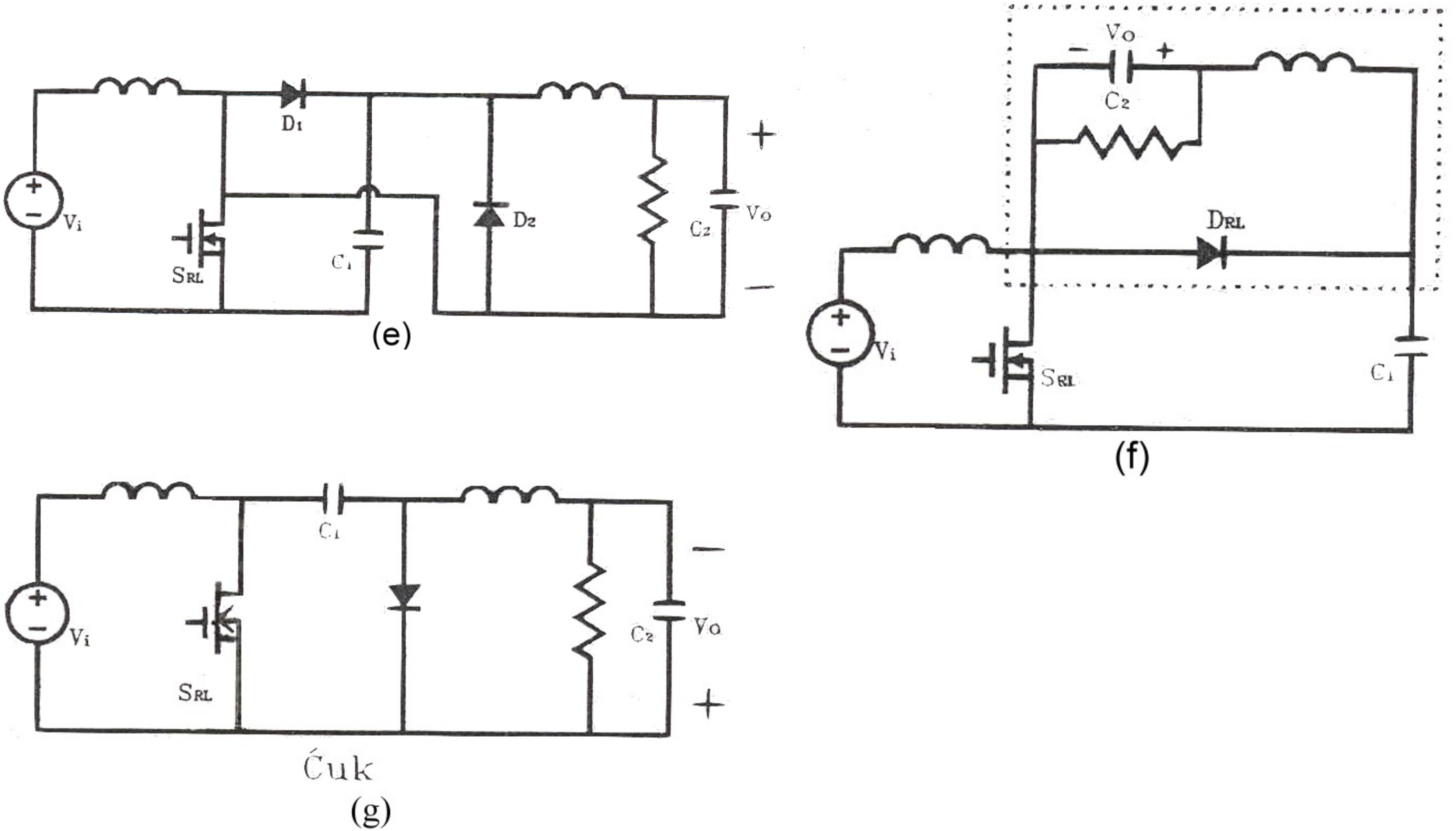
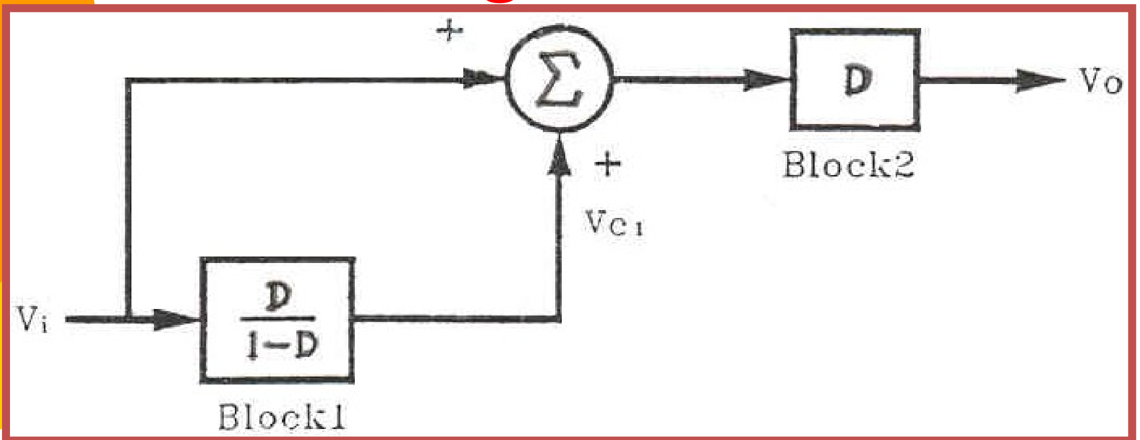


Fig. 16. (continued)

Illustration of Buck-Boost-Buck (Zeta) Integration



(a)

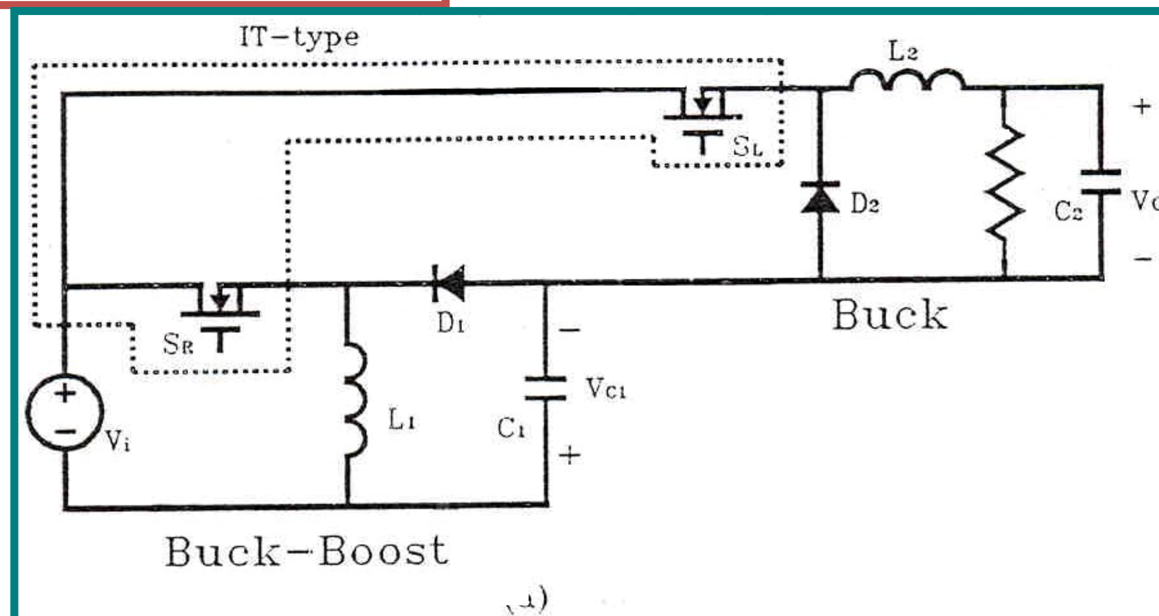


Fig. 17.

(b)

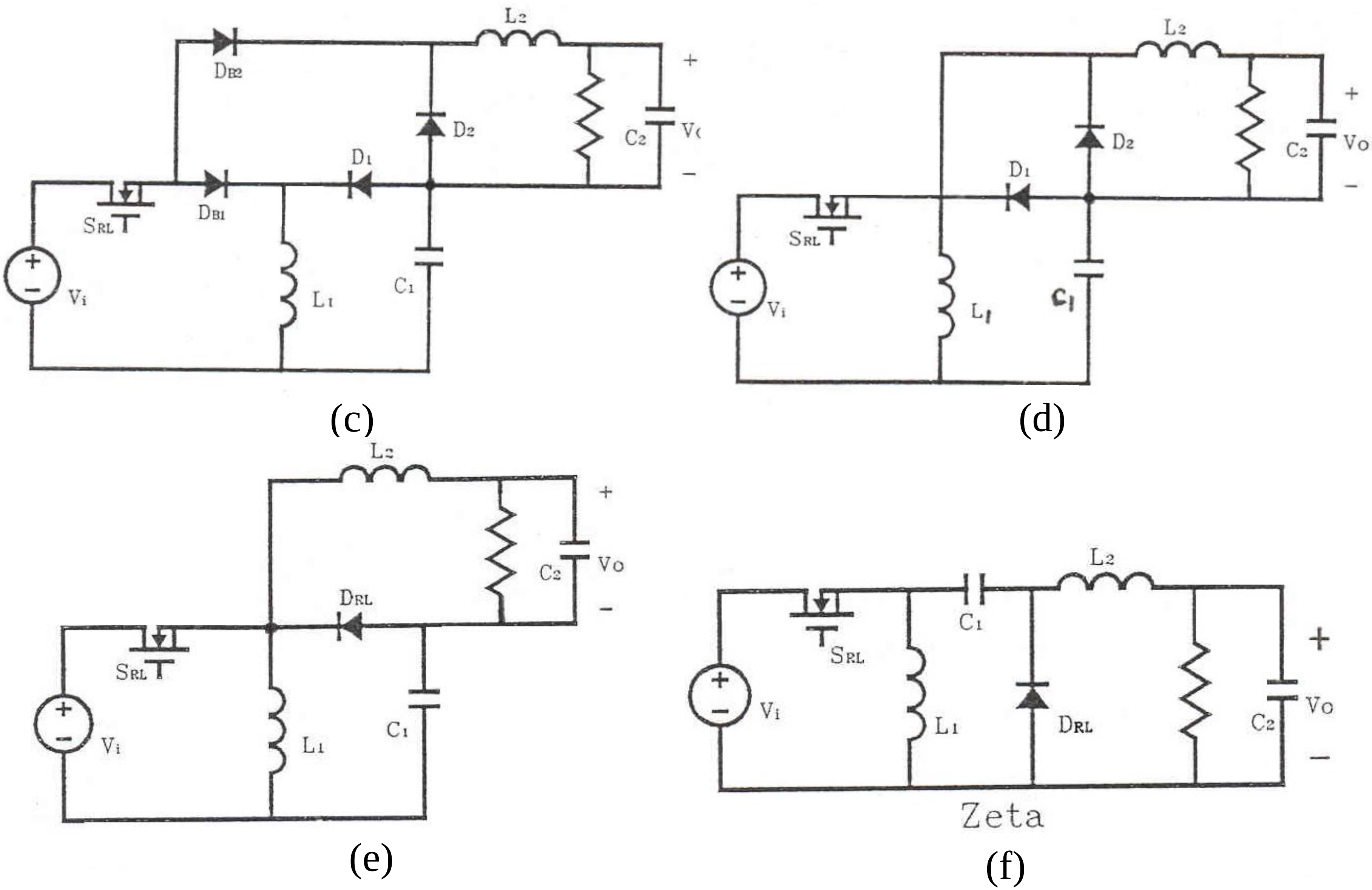


Fig. 17. (continued)

Illustration of Boost-Buck-Boost (SEPIC) Integration

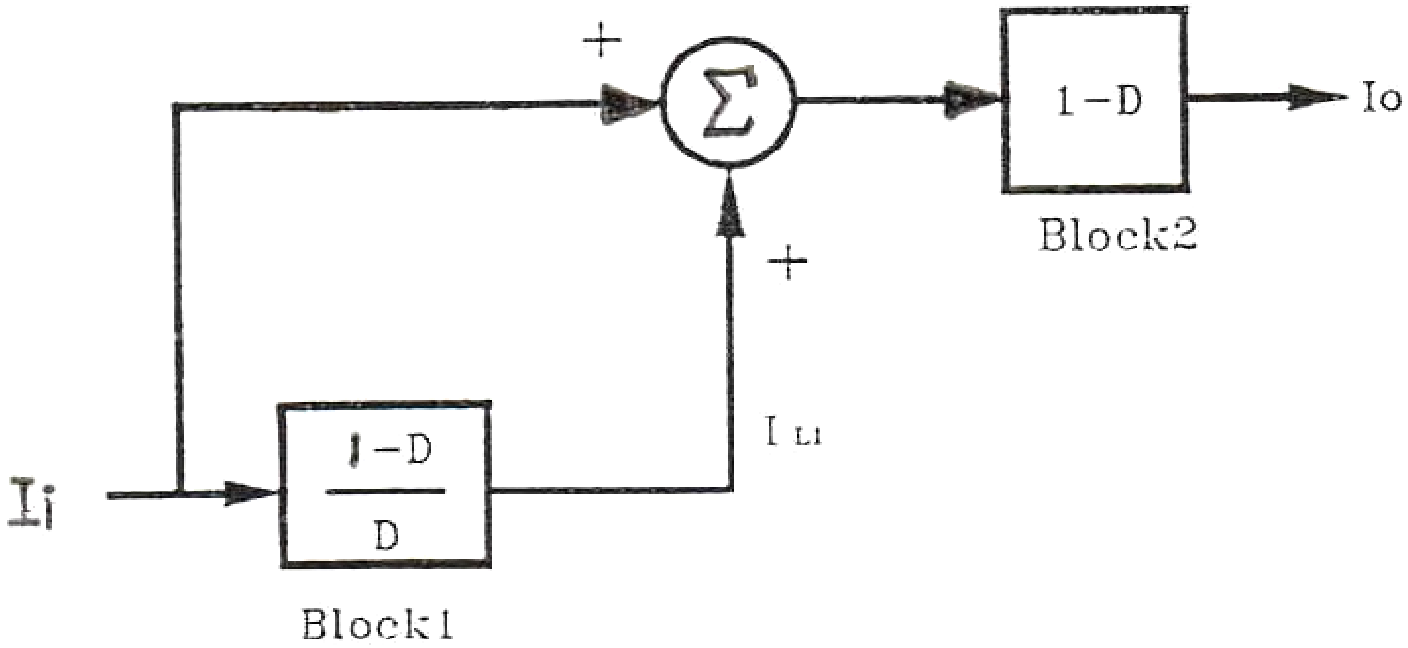


Fig. 18.

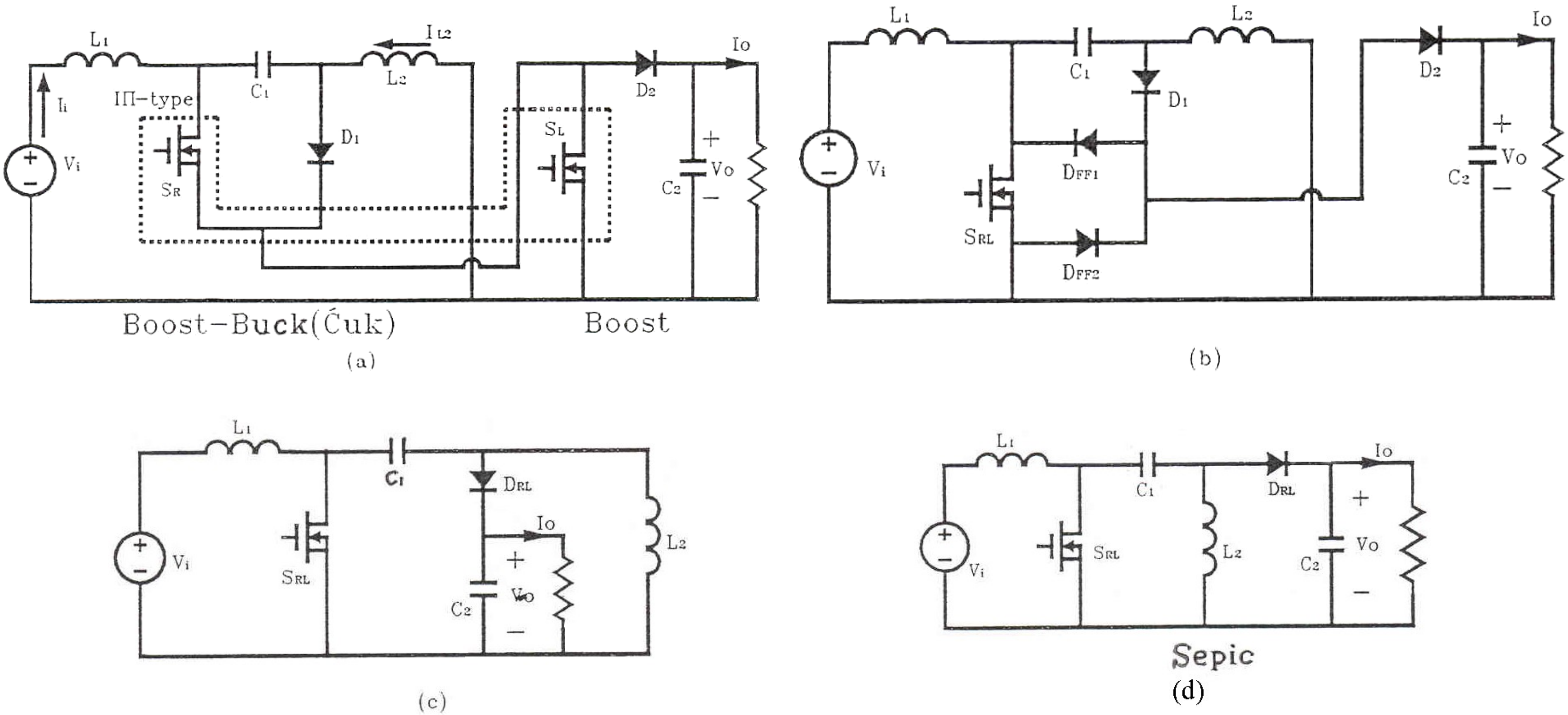
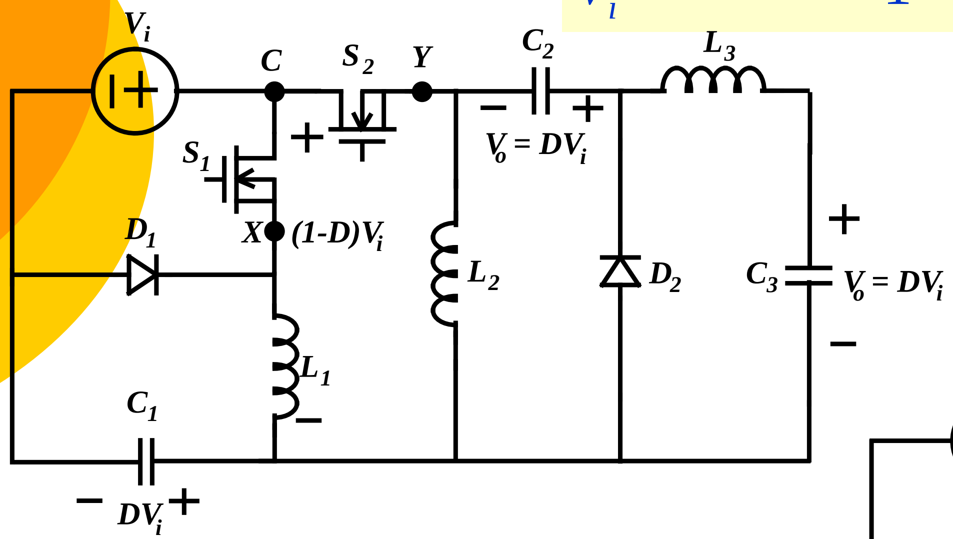


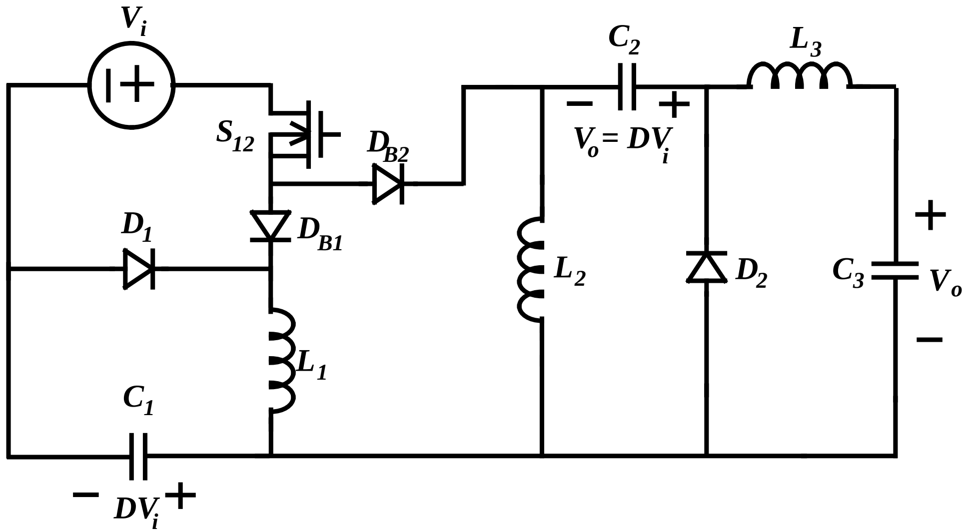
Fig. 18. (continued)

Illustrations

$$\frac{V_o}{V_i} = (1-D)\cdot\frac{D}{1-D} = D$$



(A)



(B)

Fig. 19.

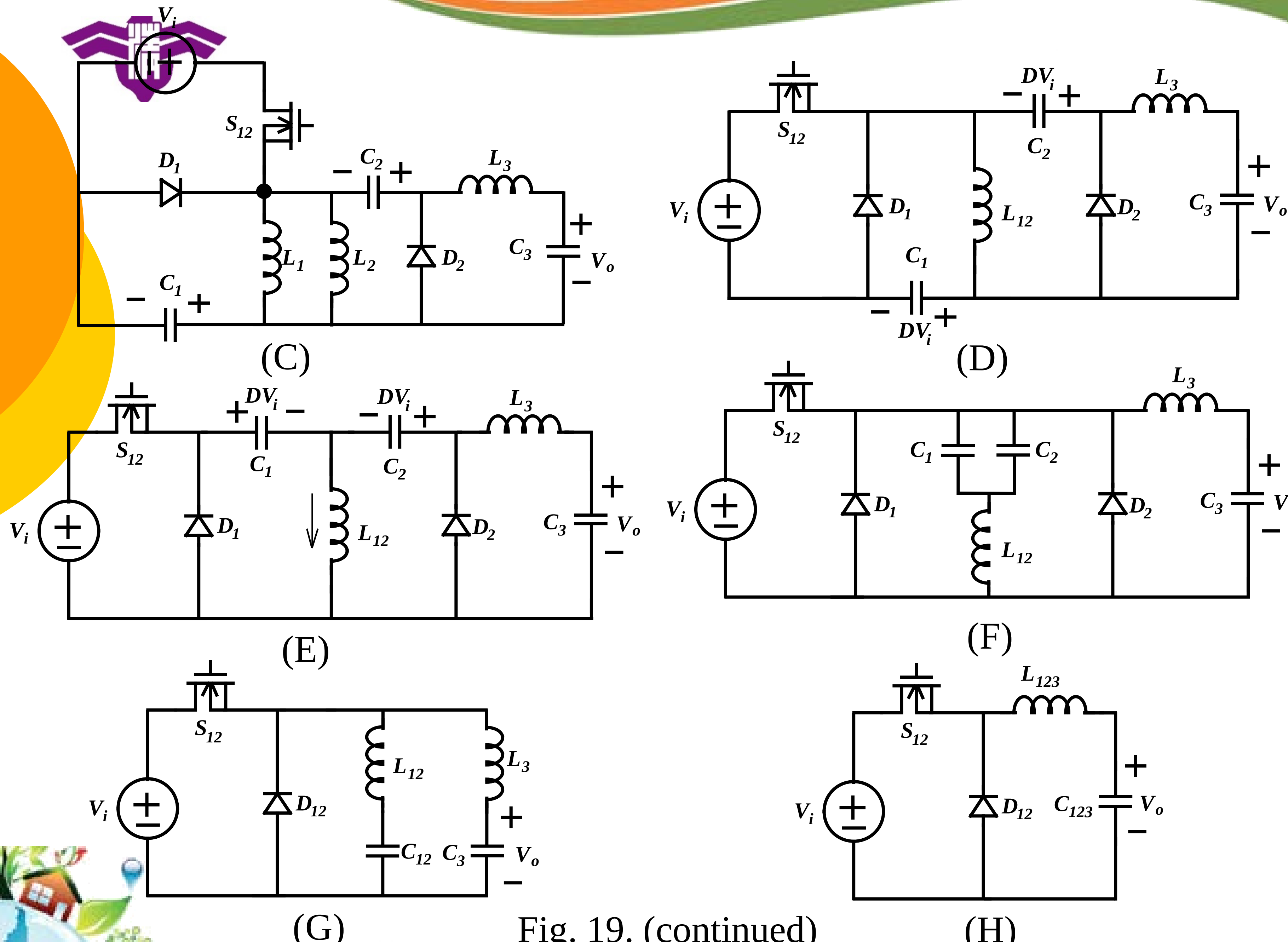


Fig. 19. (continued)

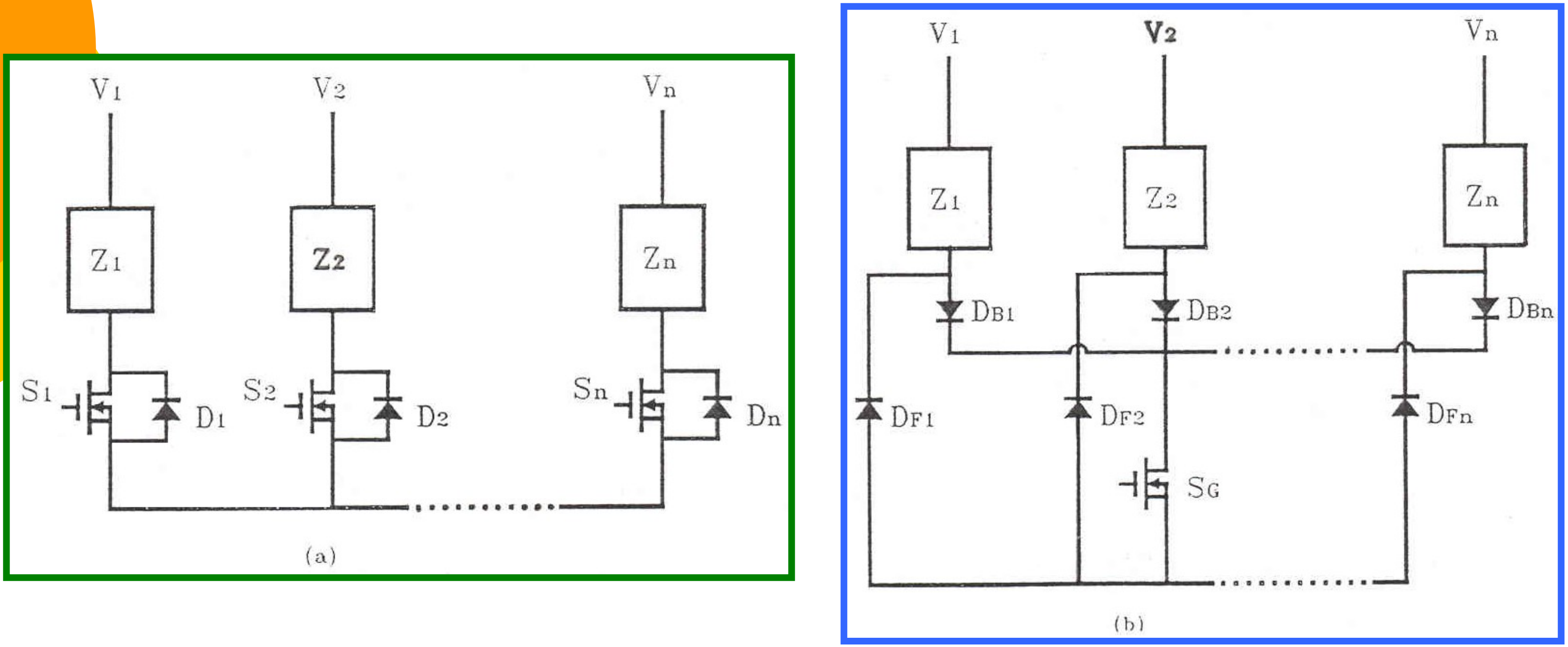
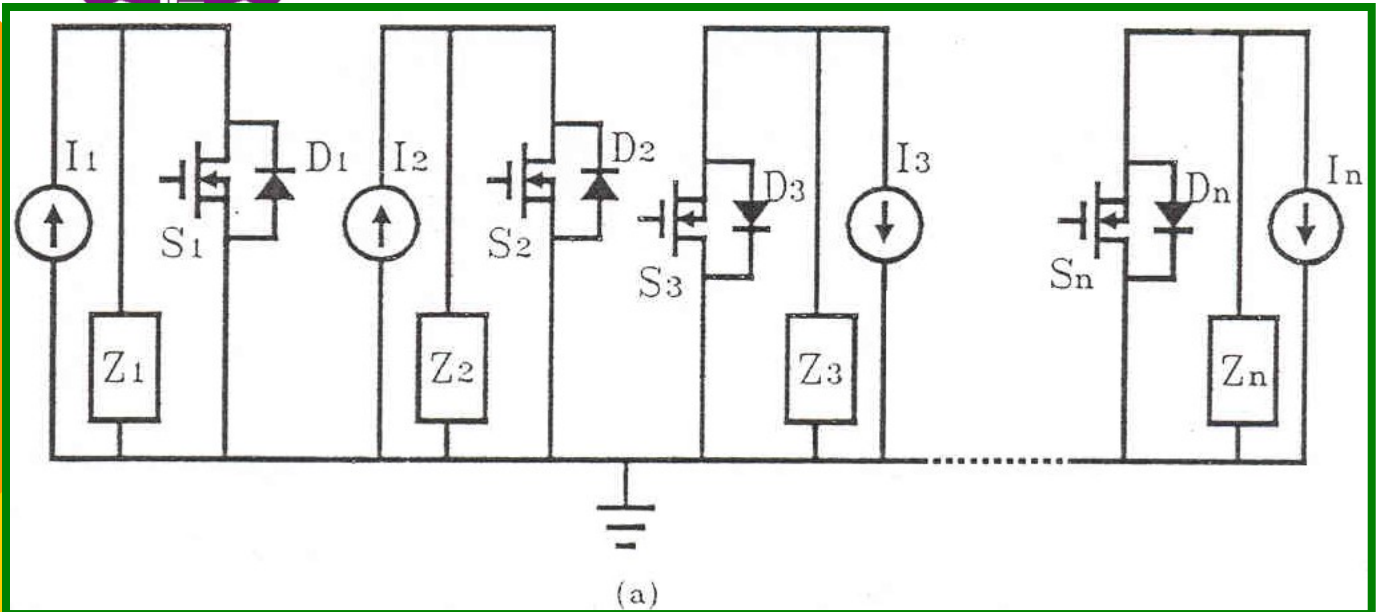

V1
V2
Vn
Z1
Z2
Zn
S1
D1
S2
D2
Sn
Dn
(a)
V1
V2
Vn
Z1
Z2
Zn
DB1
DB2
DBn
DF1
DF2
DFn
SG
(b)

Fig. 20.


I_1
D_1
S_1
Z_1
I_2
D_2
S_2
Z_2
D_3
S_3
Z_3
I_3
D_n
S_n
Z_n
I_n
(a)

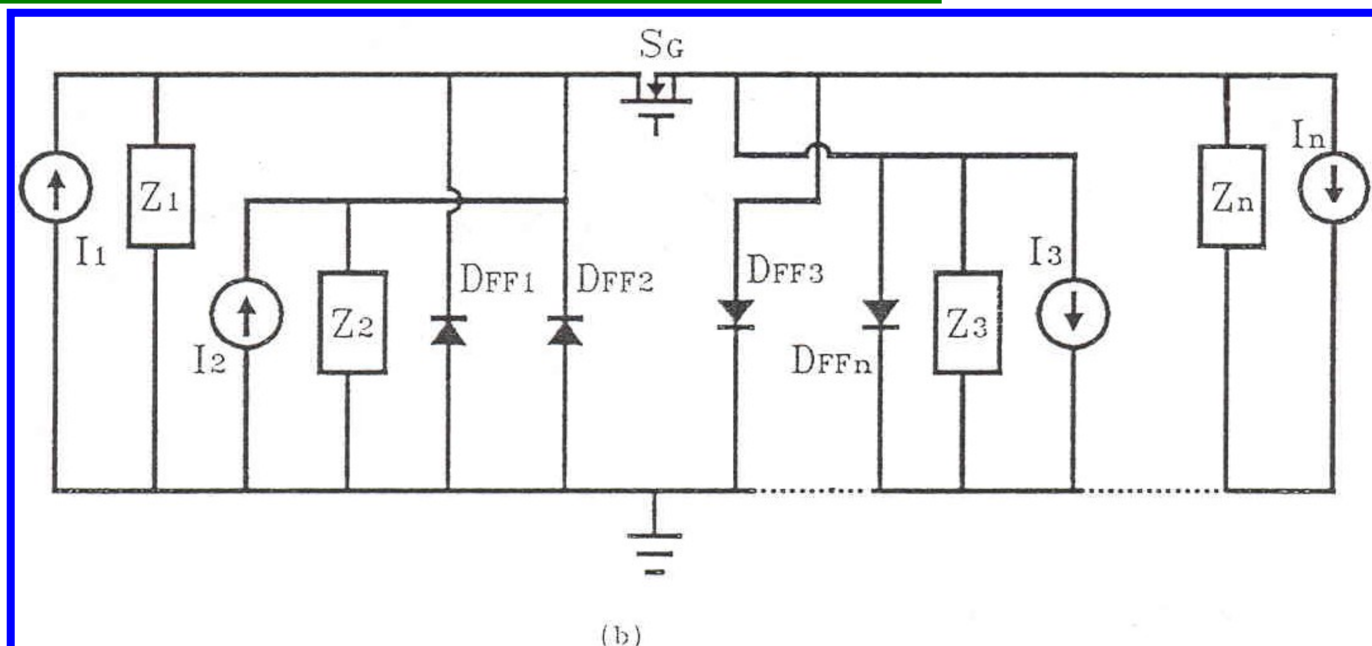

S_G
I_1
Z_1
I_2
Z_2
D_{FF1}
D_{FF2}
D_{FF3}
D_{FFn}
Z_3
I_3
Z_n
I_n
(b)

Fig. 21.

Another Applications with Graft Technique

- Dither Boost + Half-Bridge Inverter (Isao Takahashi)

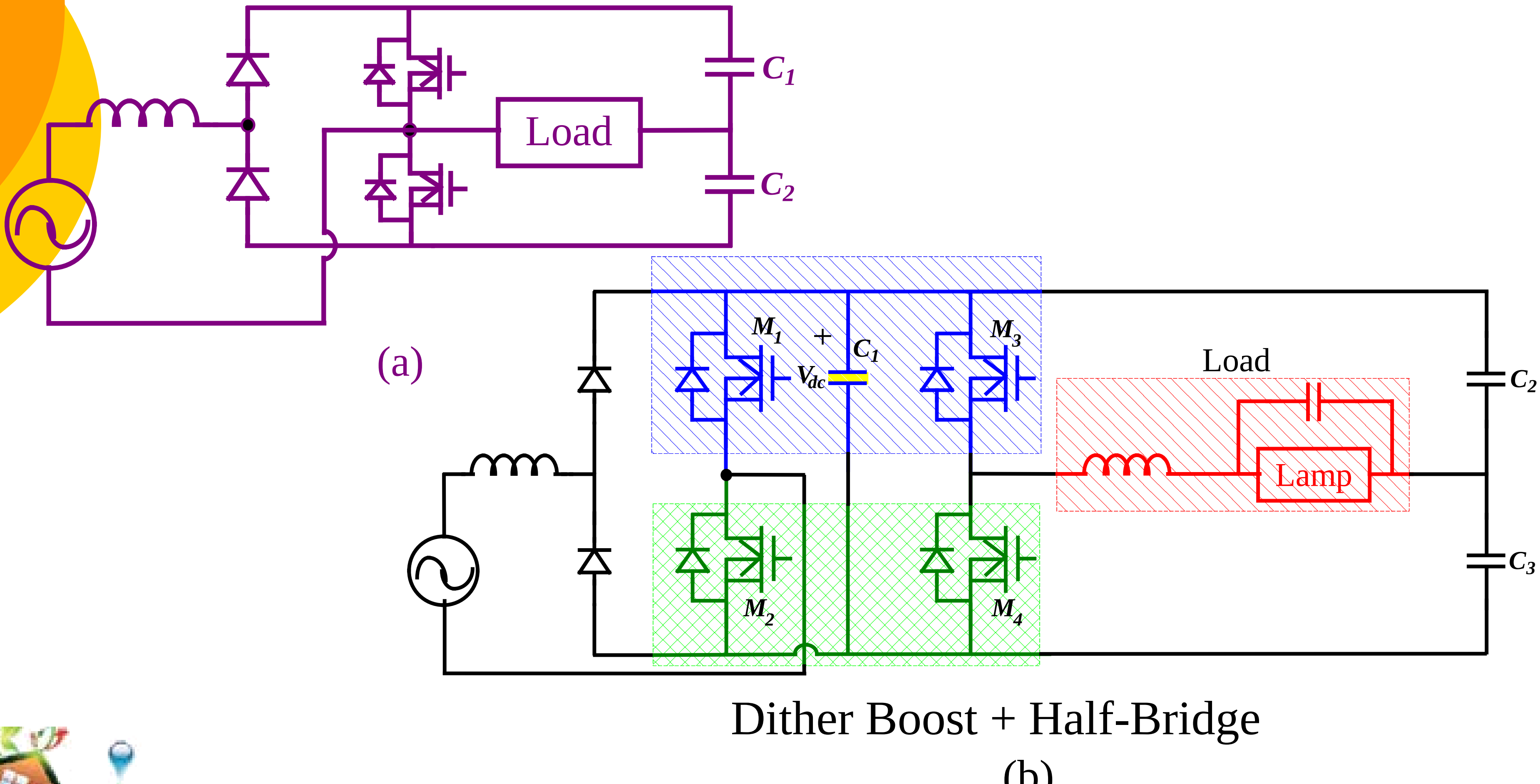
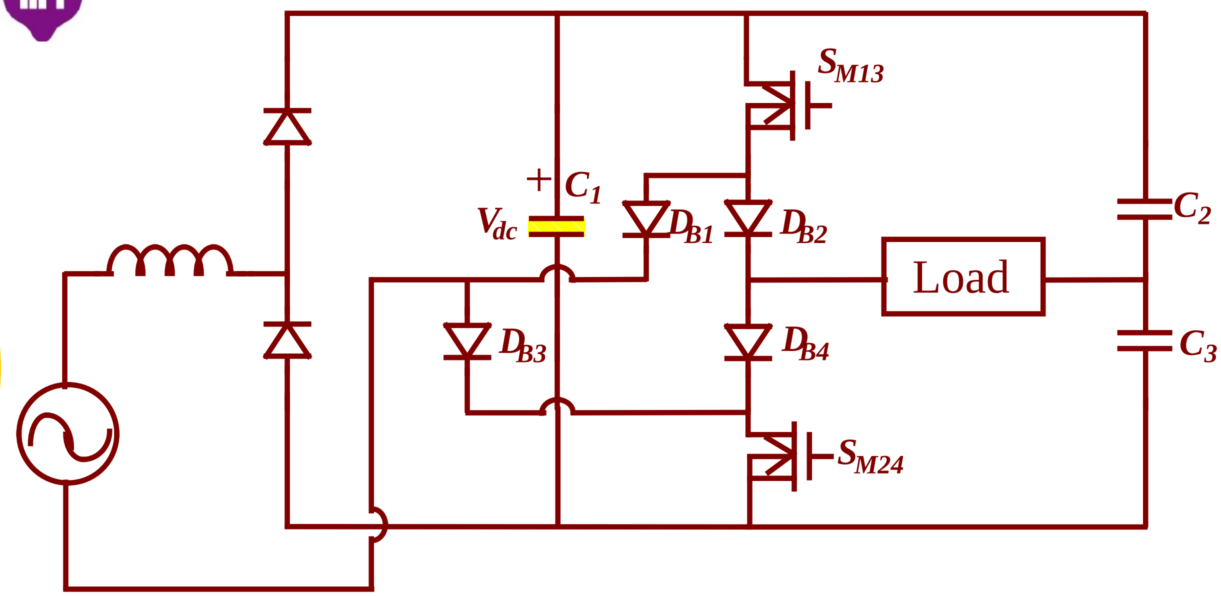
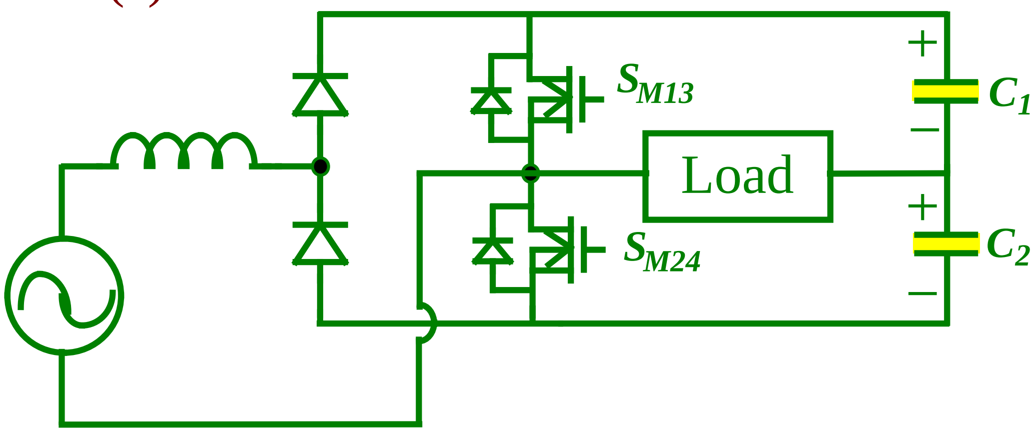


Fig. 22.



(c)



(d)

Fig. 22. (continued)

➢ 3-in-1 Converter (Charger + Discharger + Ballast)

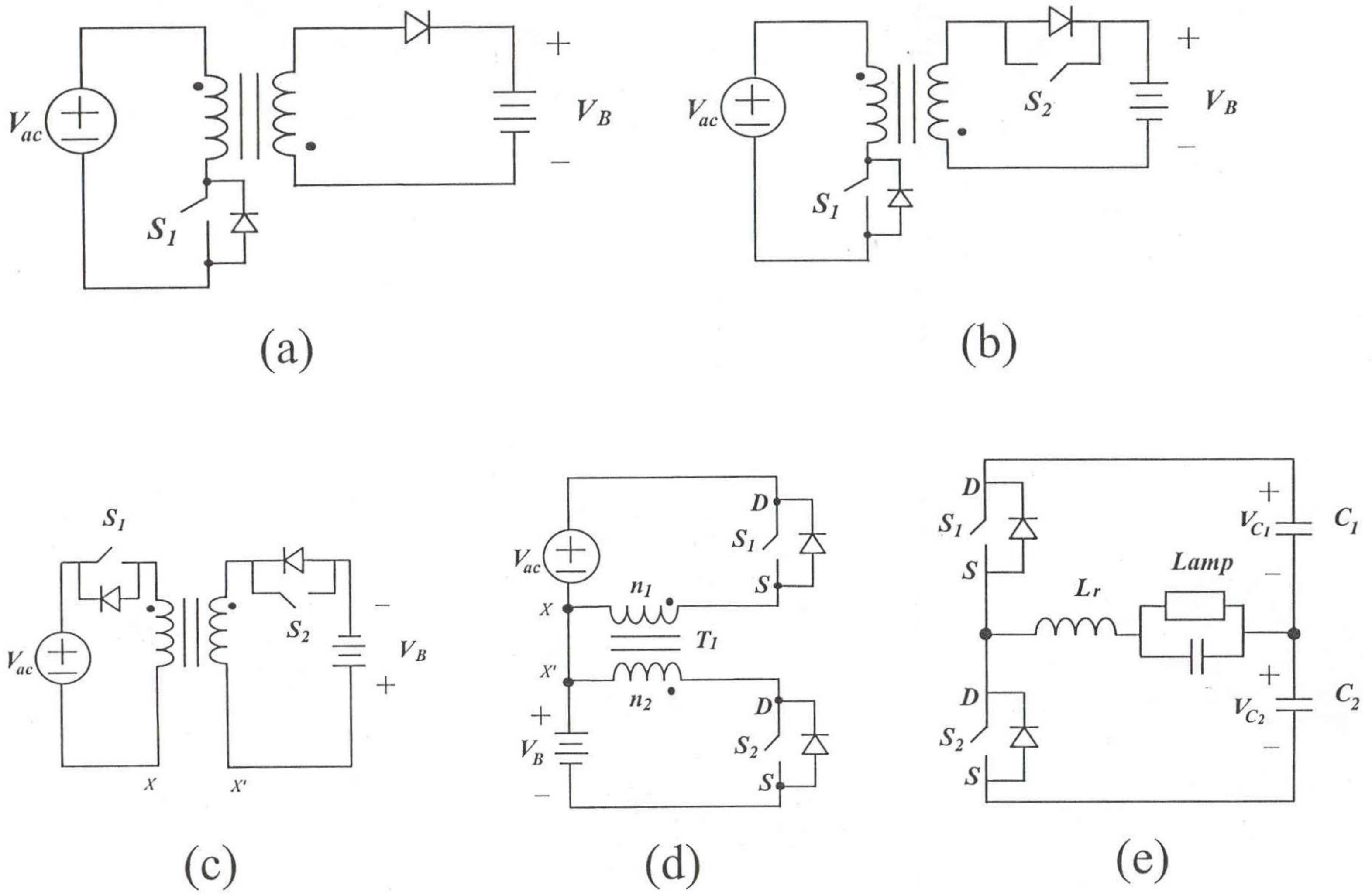
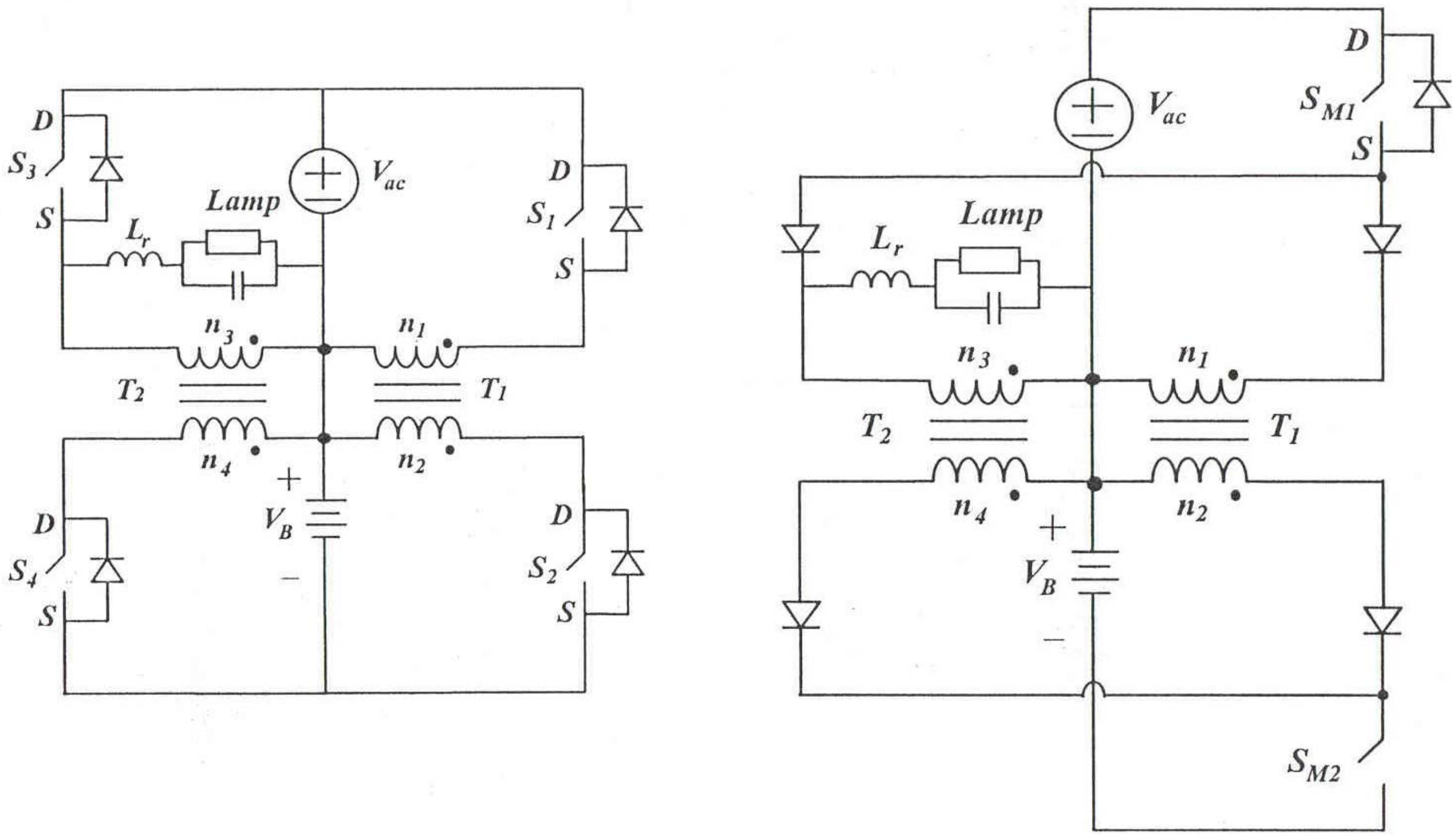
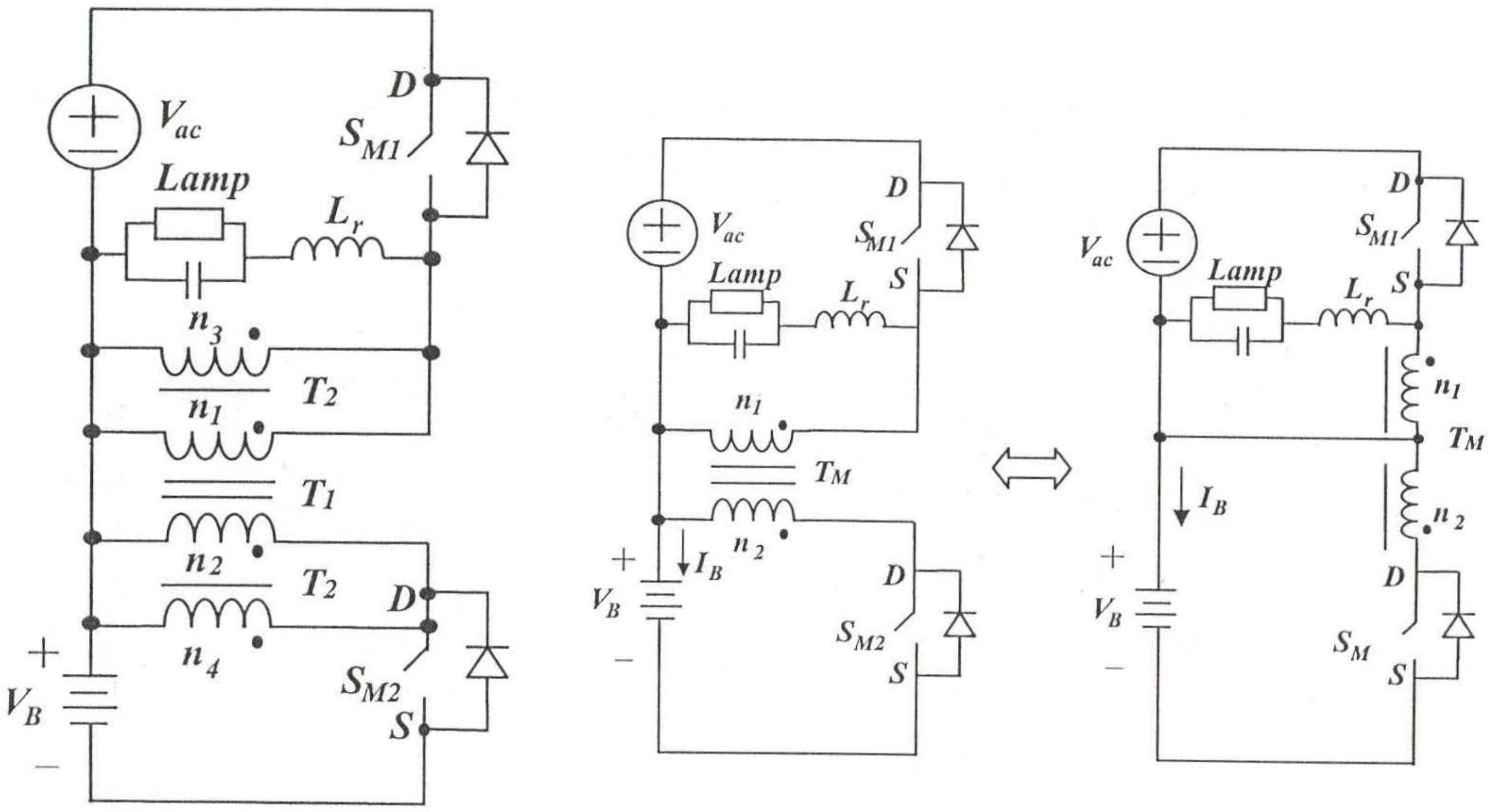


Fig. 23.



(f) (g)

Fig. 23. (continued)



(h) (i)

Fig. 23. (continued)

Boost + Half Bridge (Ćuk)

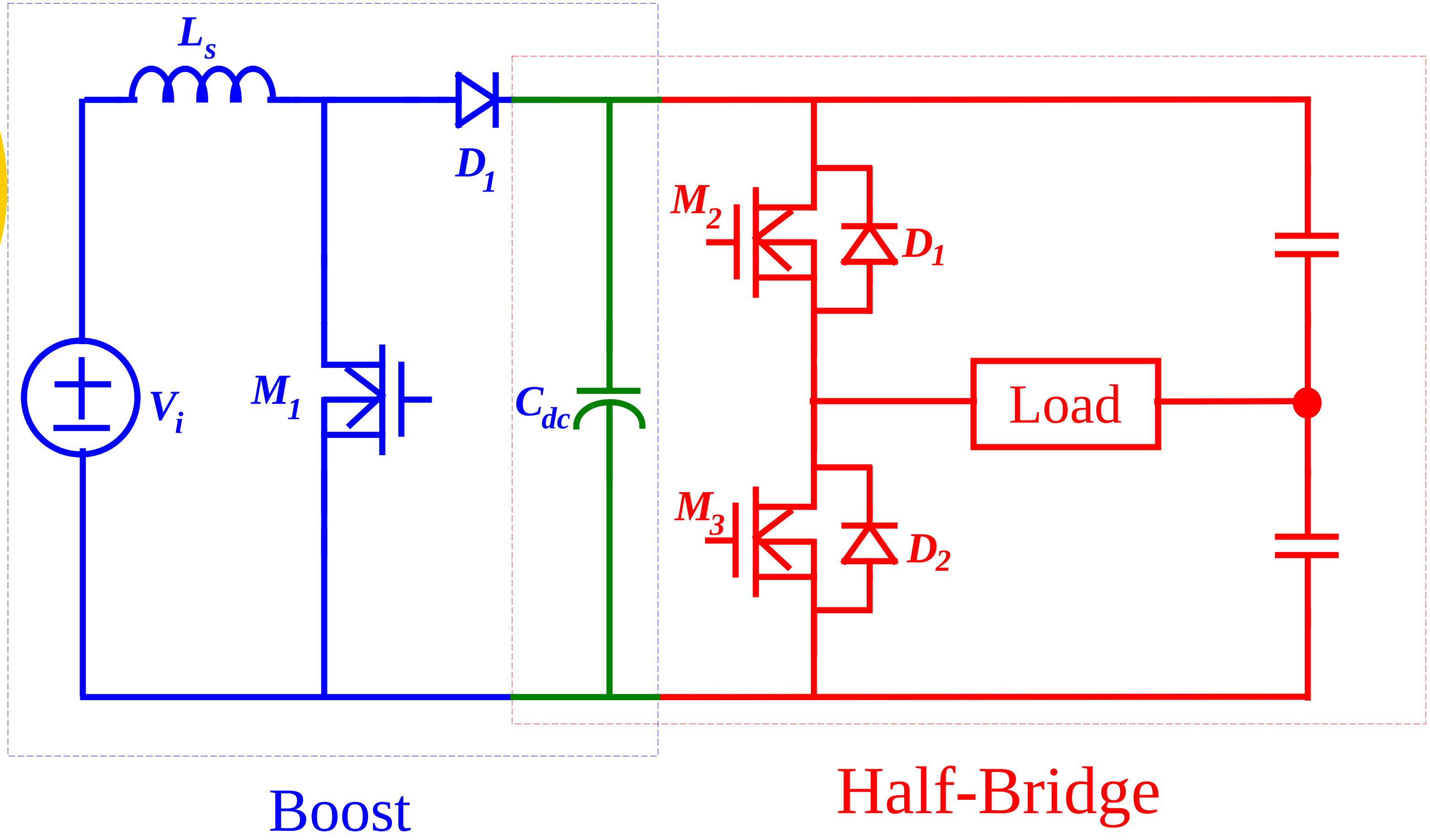


Fig. 24.

Switches M_1 and M_3 are sharing a common node *s*-*s* and they can operated synchronously; thus, we have the following integrated converter:

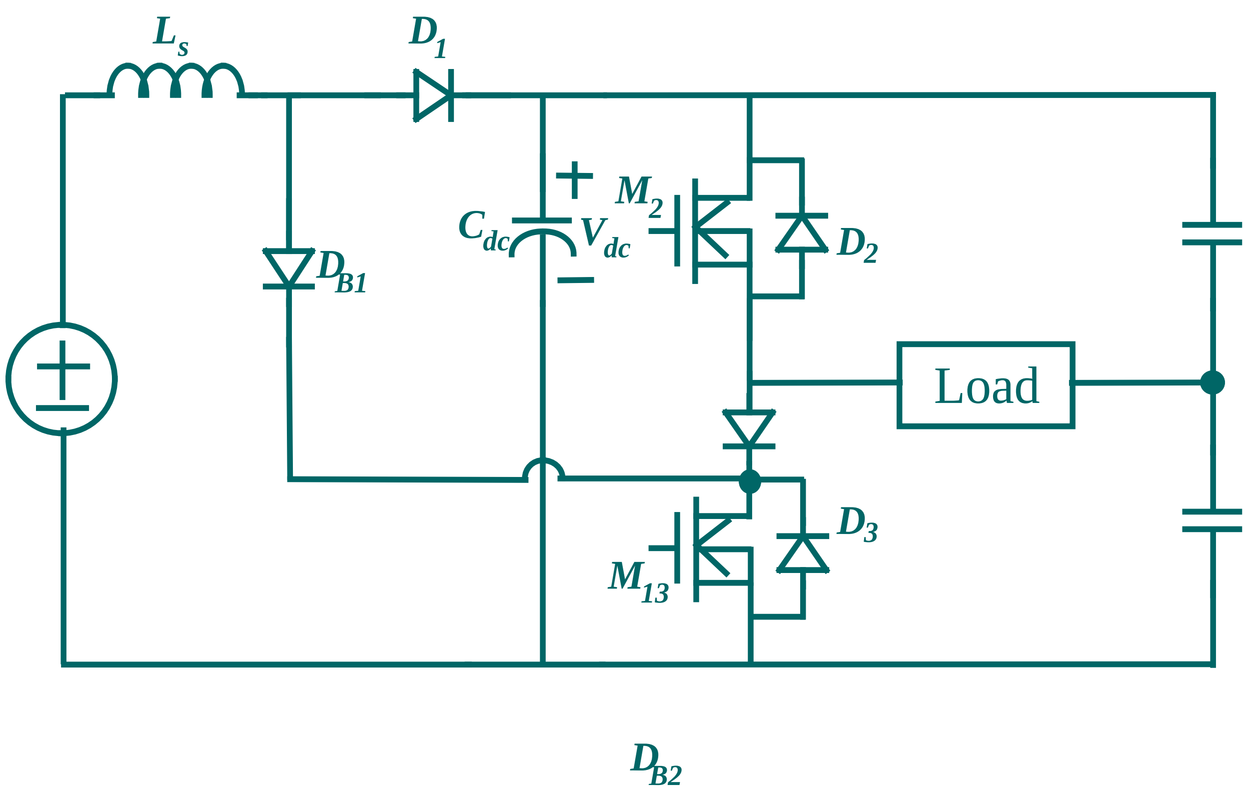


Fig. 25.

Since the voltage stresses imposed on M_1 and M_3 are the same and is V_{dc}, diodes D_{B1} and D_{B2} can be removed (*i.e.* shorted). The circuit shown in Fig. 25 can be simplified to the one shown as follows:

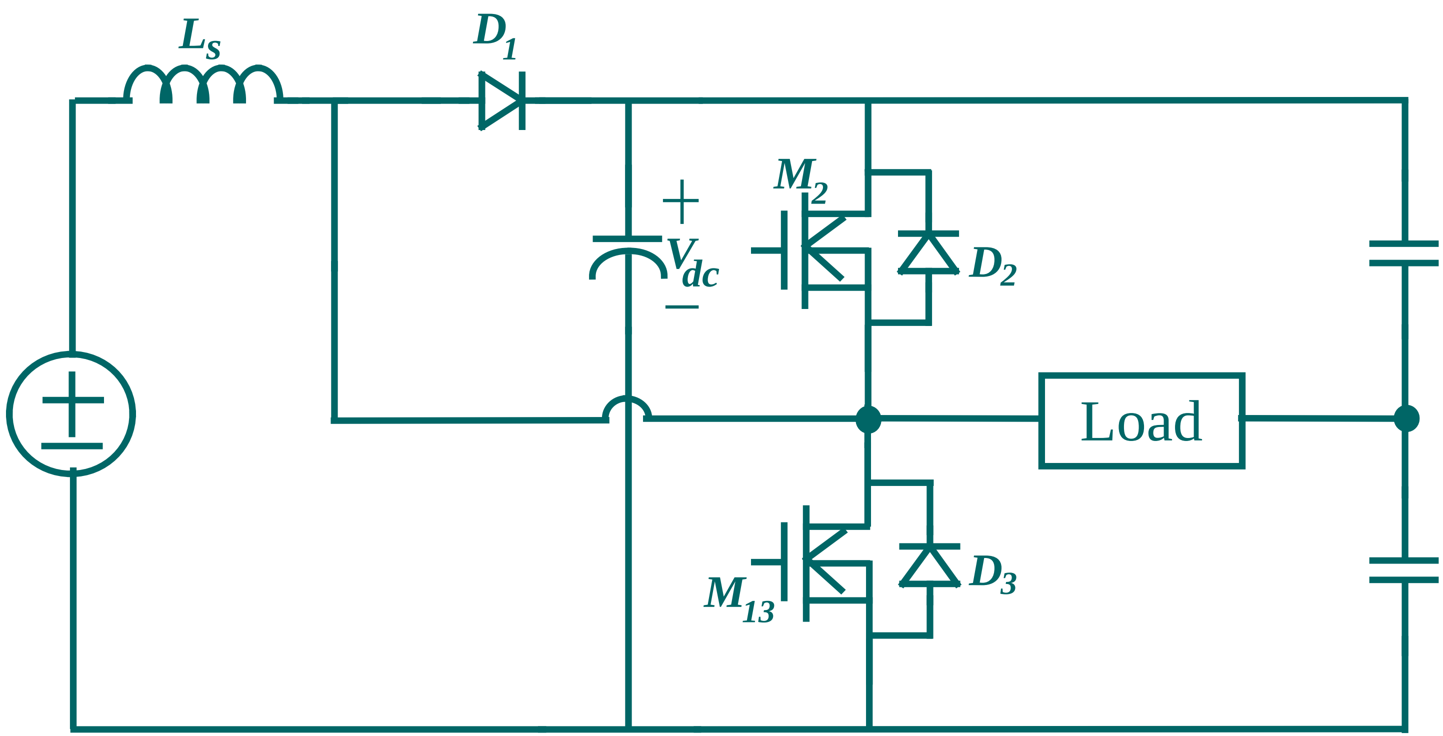
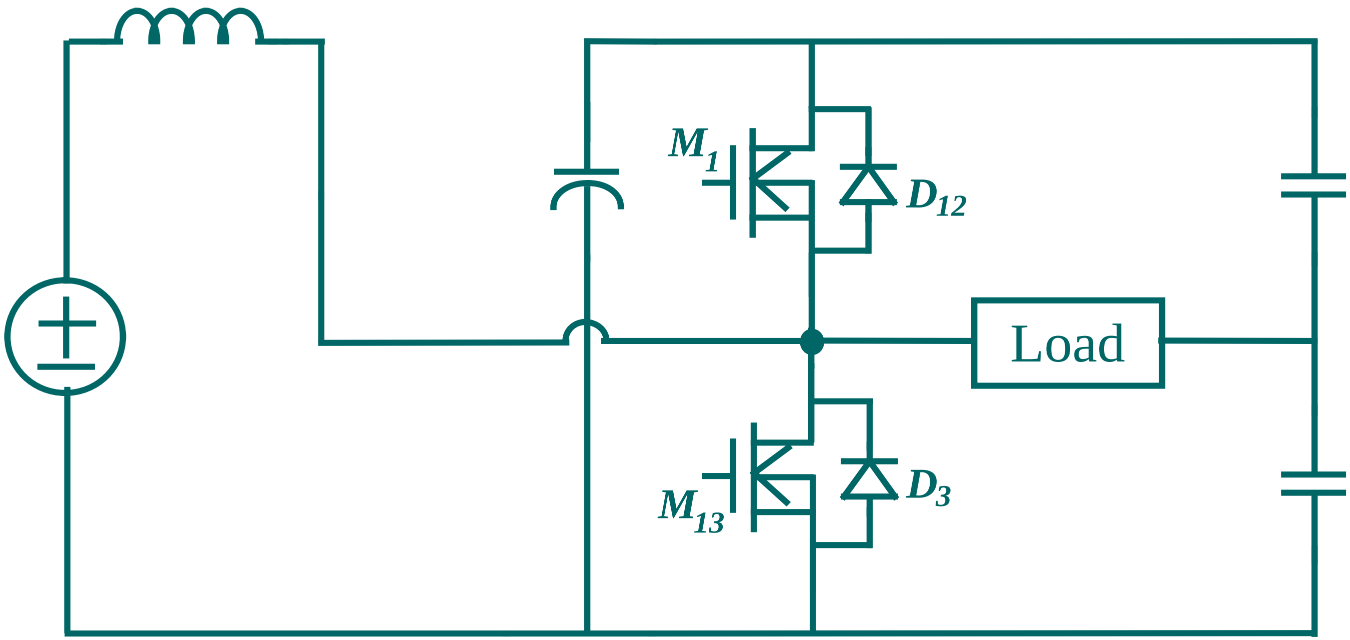


Fig. 26.

It is obvious that diodes D_1 and D_2 are in parallel. Thus, the circuit shown in Fig. 26 can be further simplified to Fig. 27.



Boost + Half-Bridge

Fig. 27.

Boost + class E (Ćuk)

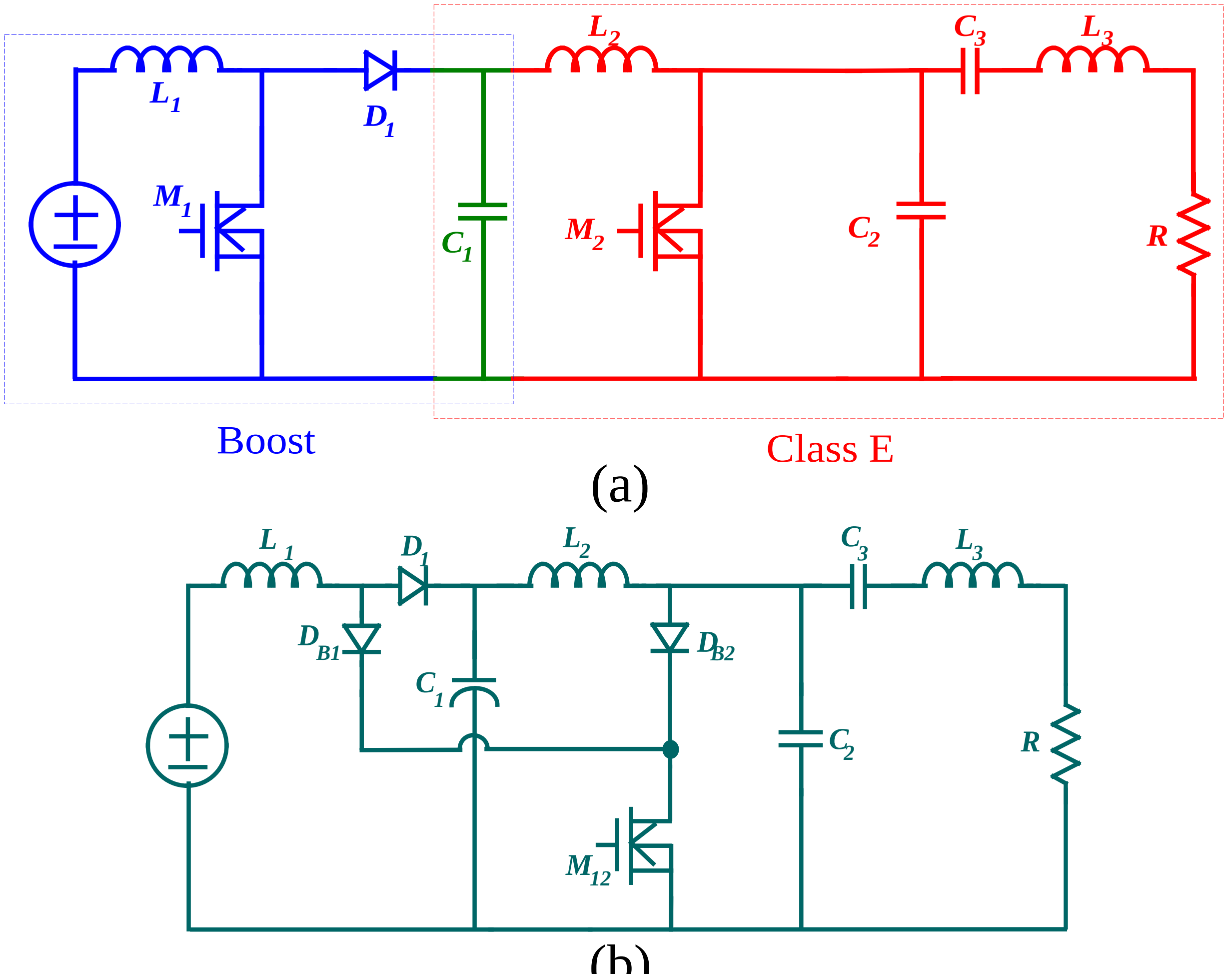
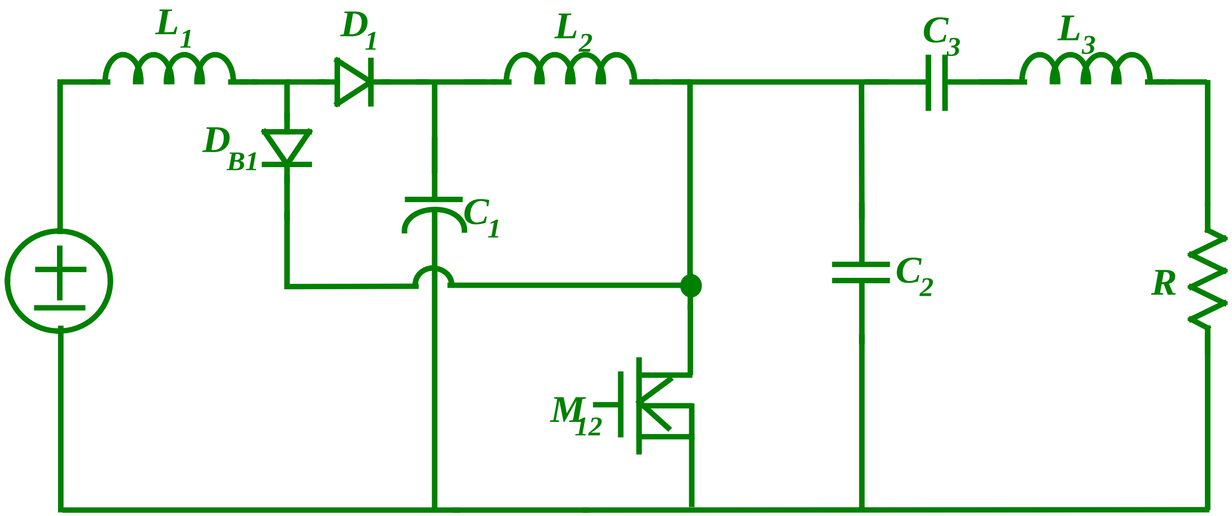


Fig. 28.

Since $V_{ds}(M_2) > V_{dc}(M_1)$ during turn-off, thus we have the following circuit:



Boost + Class E

(c)

Fig. 28. (continued)

Buck//Buck-Boost

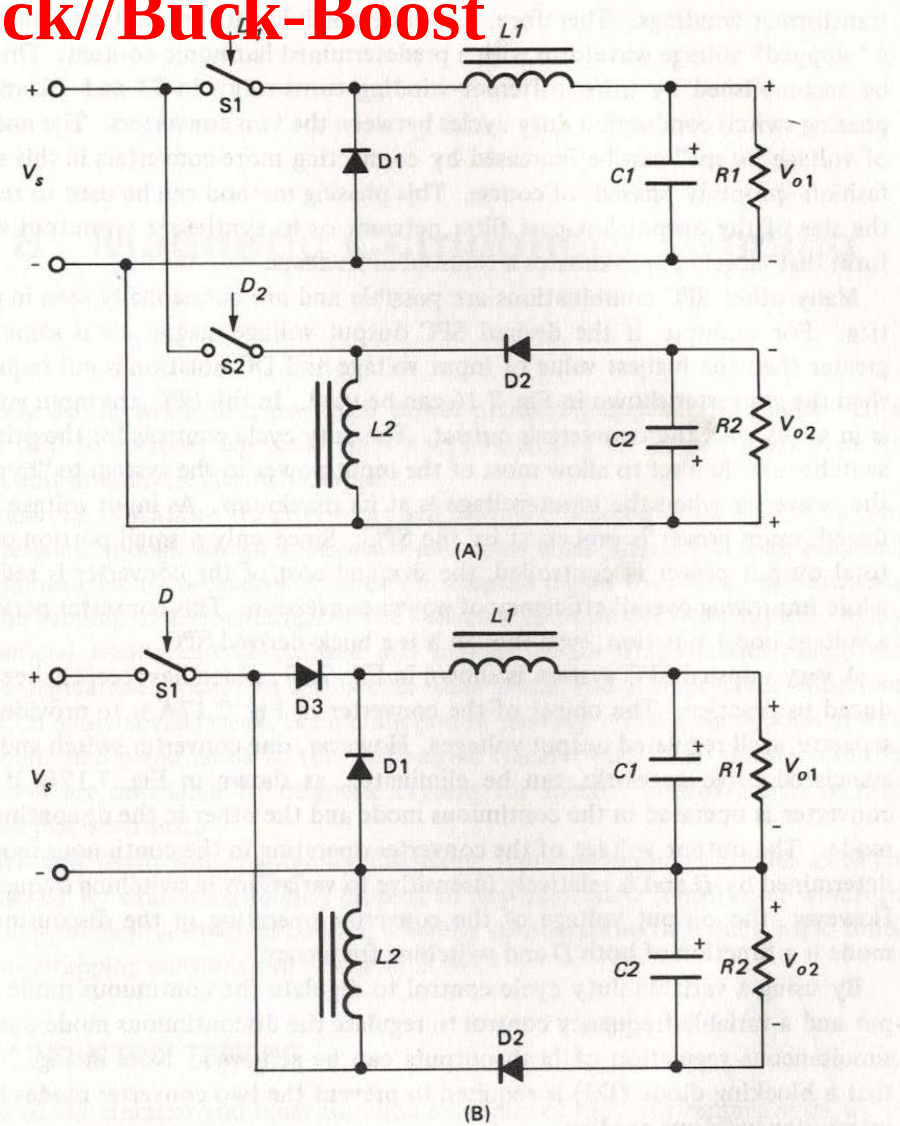
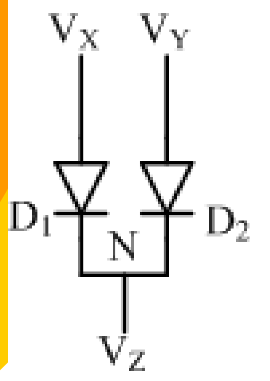
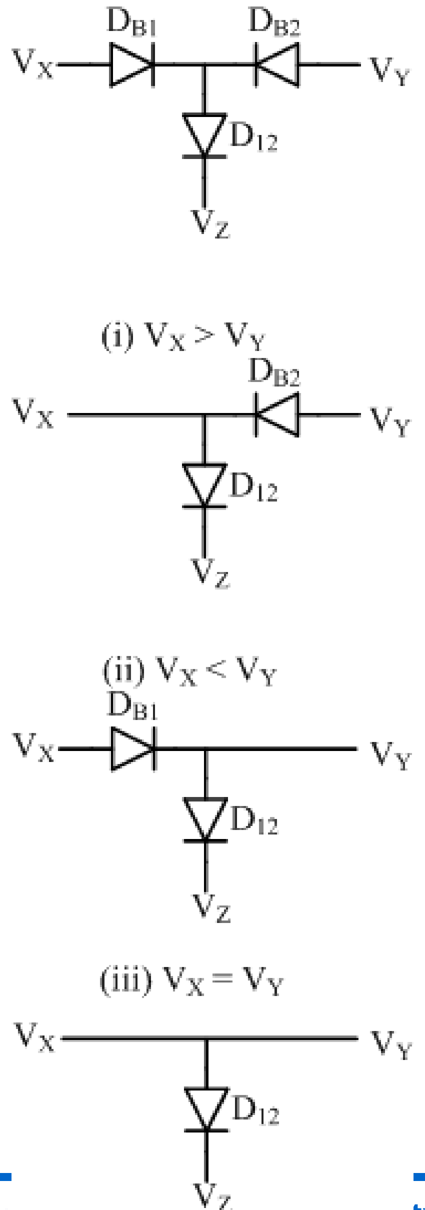


Fig. 29. A scheme for combining duty cycle and frequency modulation to provide two regulated outputs with one switch.[3]

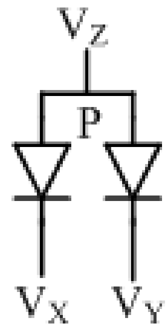
➤ with Grafted Diodes



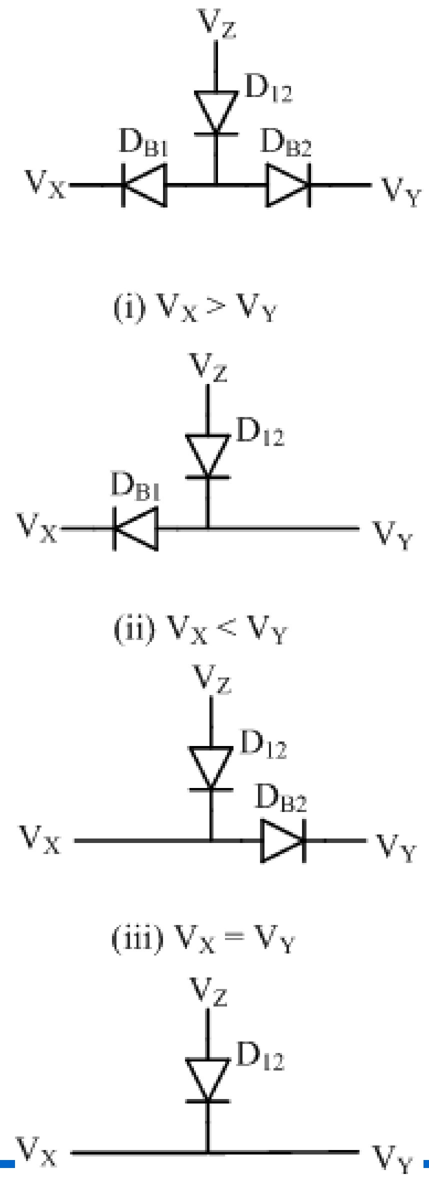
(a) Common N-N



(b)



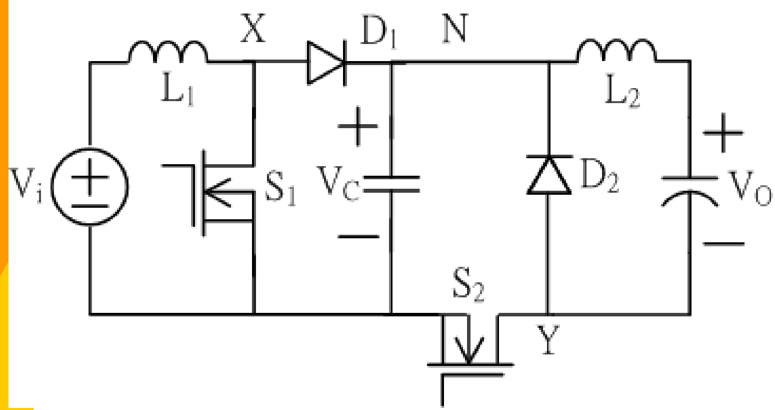
(c) Common P-P



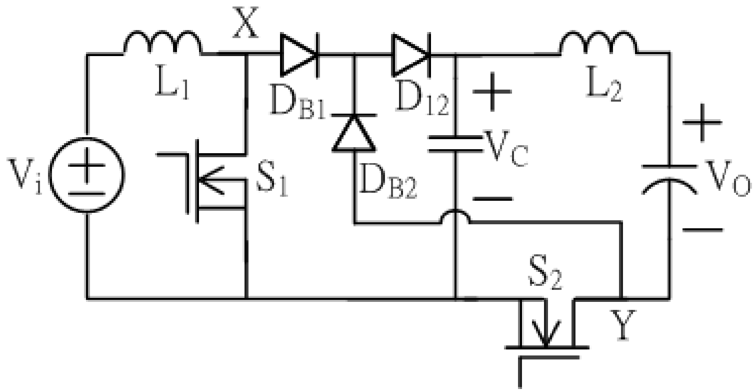
(d)

Fig. 30.

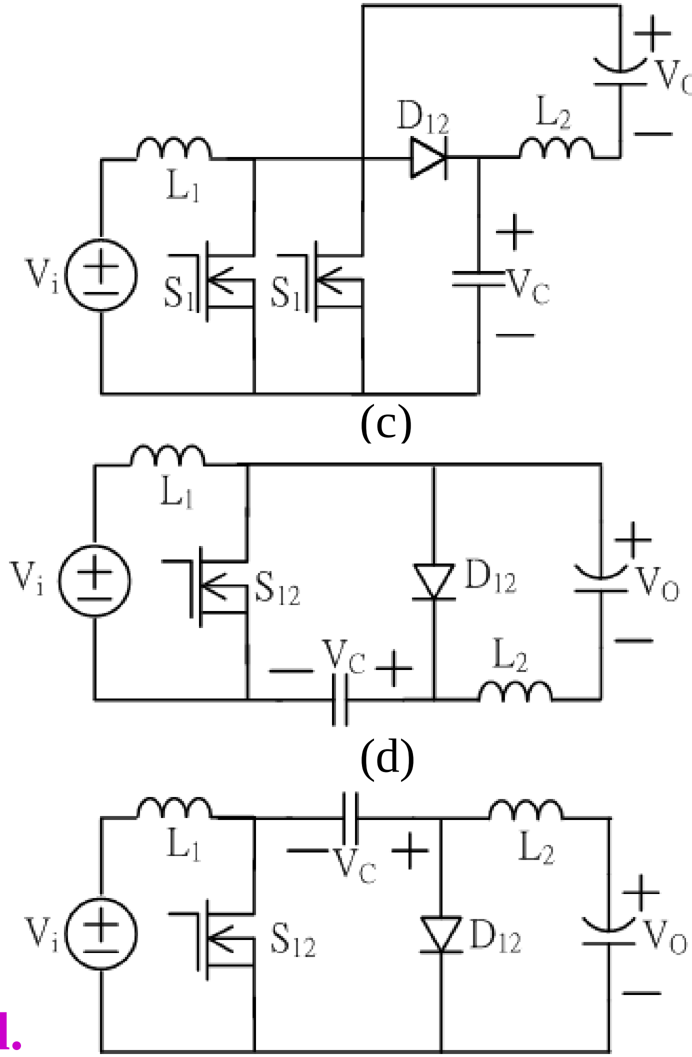
➢ Illustration of Boost + Buck with Grafted Diodes



(a) Boost+Buck



(b)



(c)

(d)

Since V_X=V_Y, D_{B1} and D_{B2} can be shorted.

Fig. 31. (e) Ćuk (Boost-Buck)

V. Layer Scheme

- Derivation of Buck-Boost and Zeta Converters

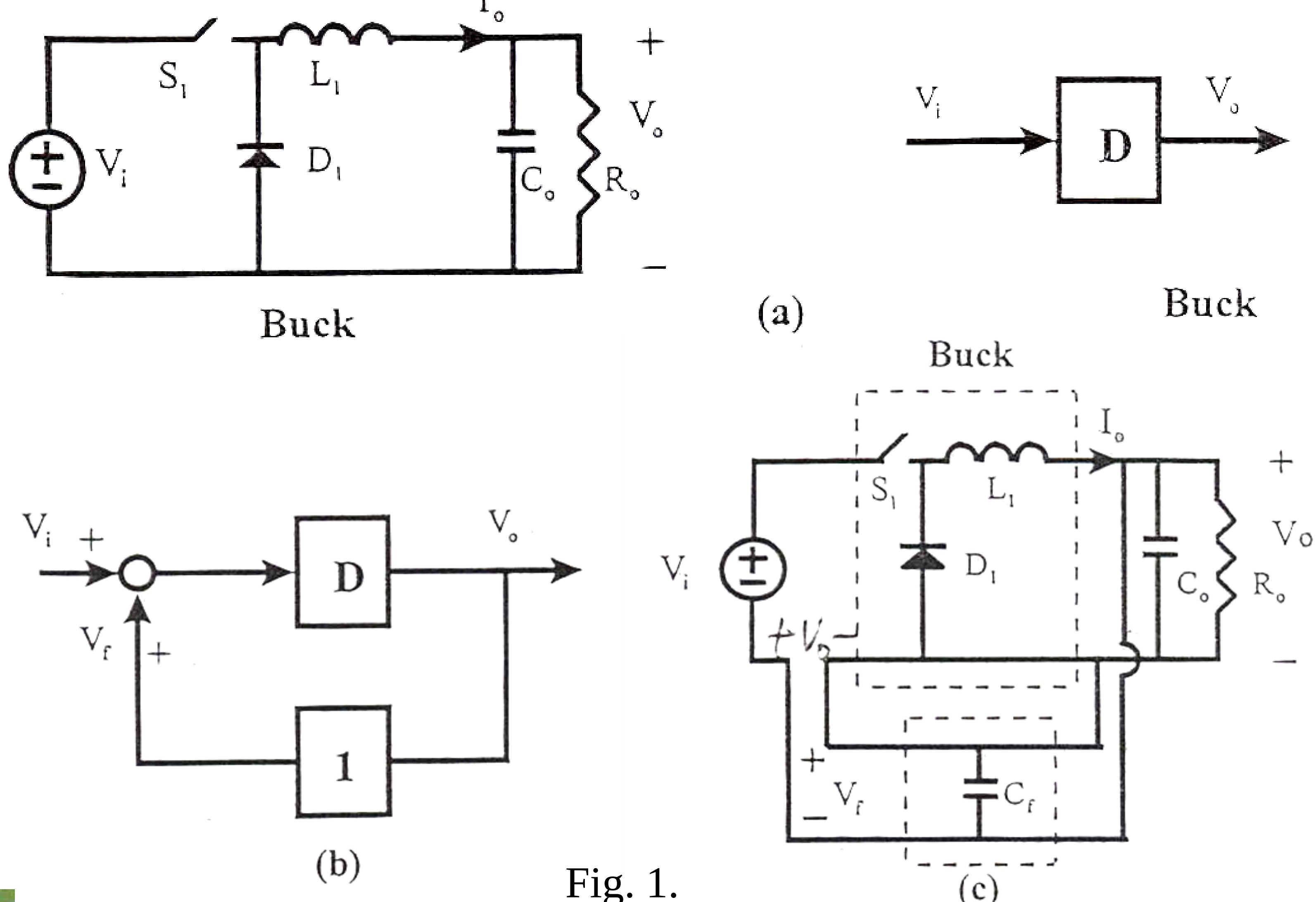
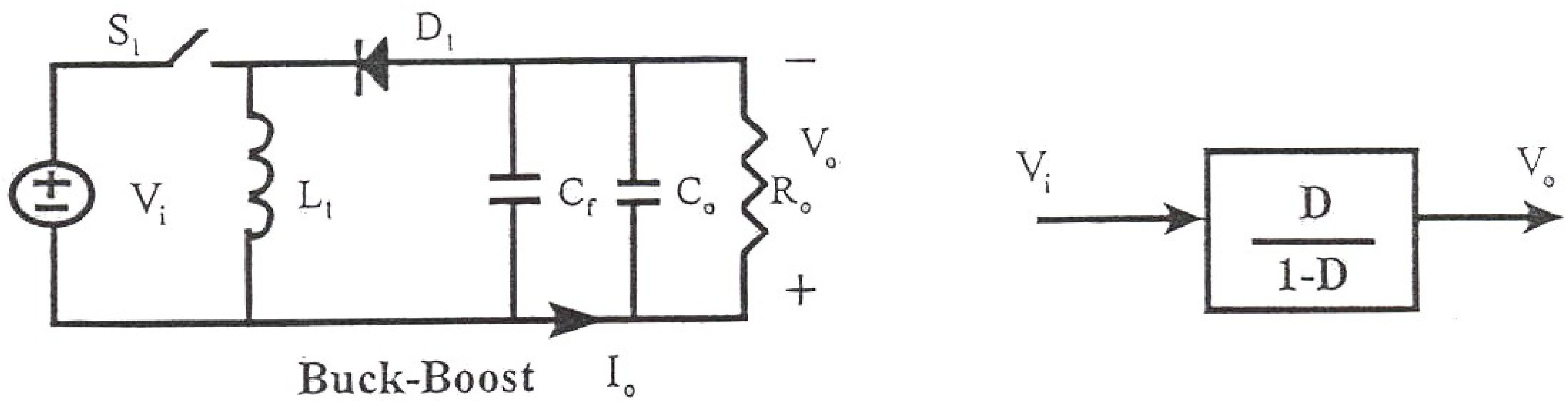
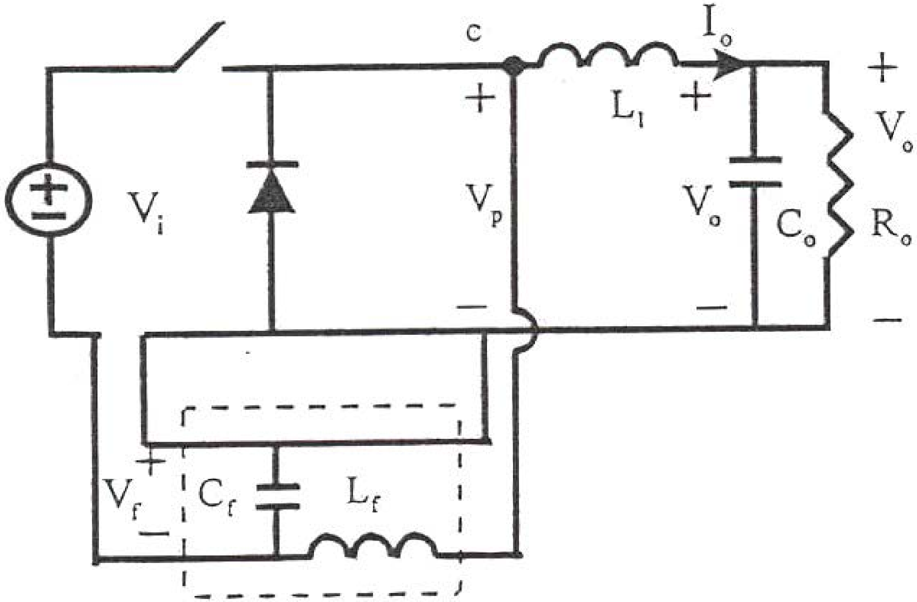


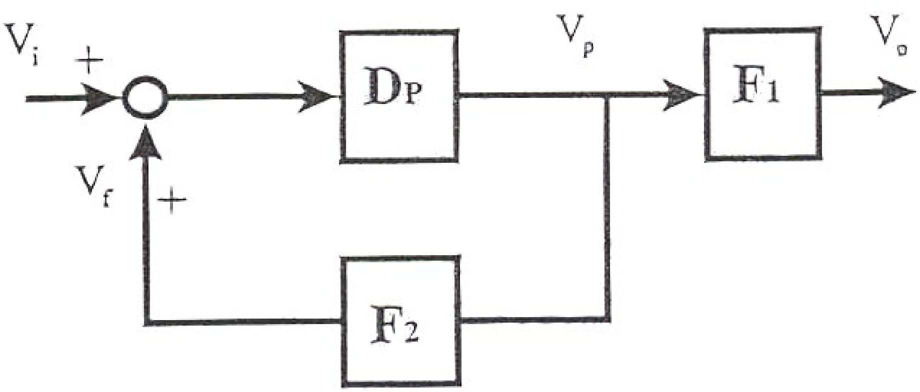
Fig. 1.



(d)



(e)



(f)

Fig. 1. (continued)

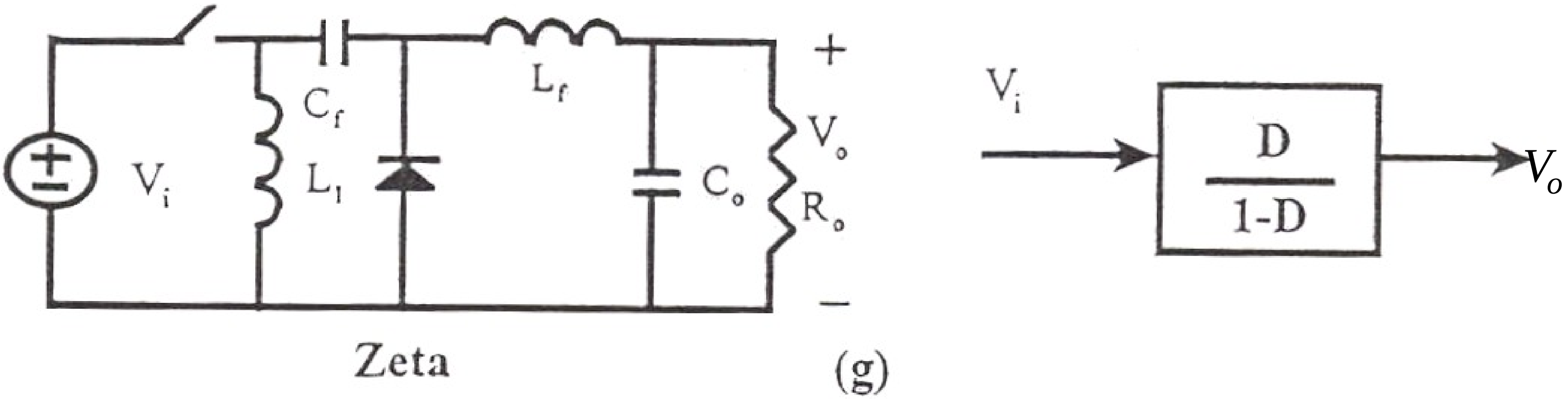


Fig. 1. (continued)

$$\frac{V_o}{V_i} = \frac{D_p F_1}{1 - D_p F_2}$$

Let $F_1 = F_2$,

at dc,

$$\frac{V_o}{V_i} = \frac{D}{1 - D}.$$

Derivation of Ćuk and Sepic Converters

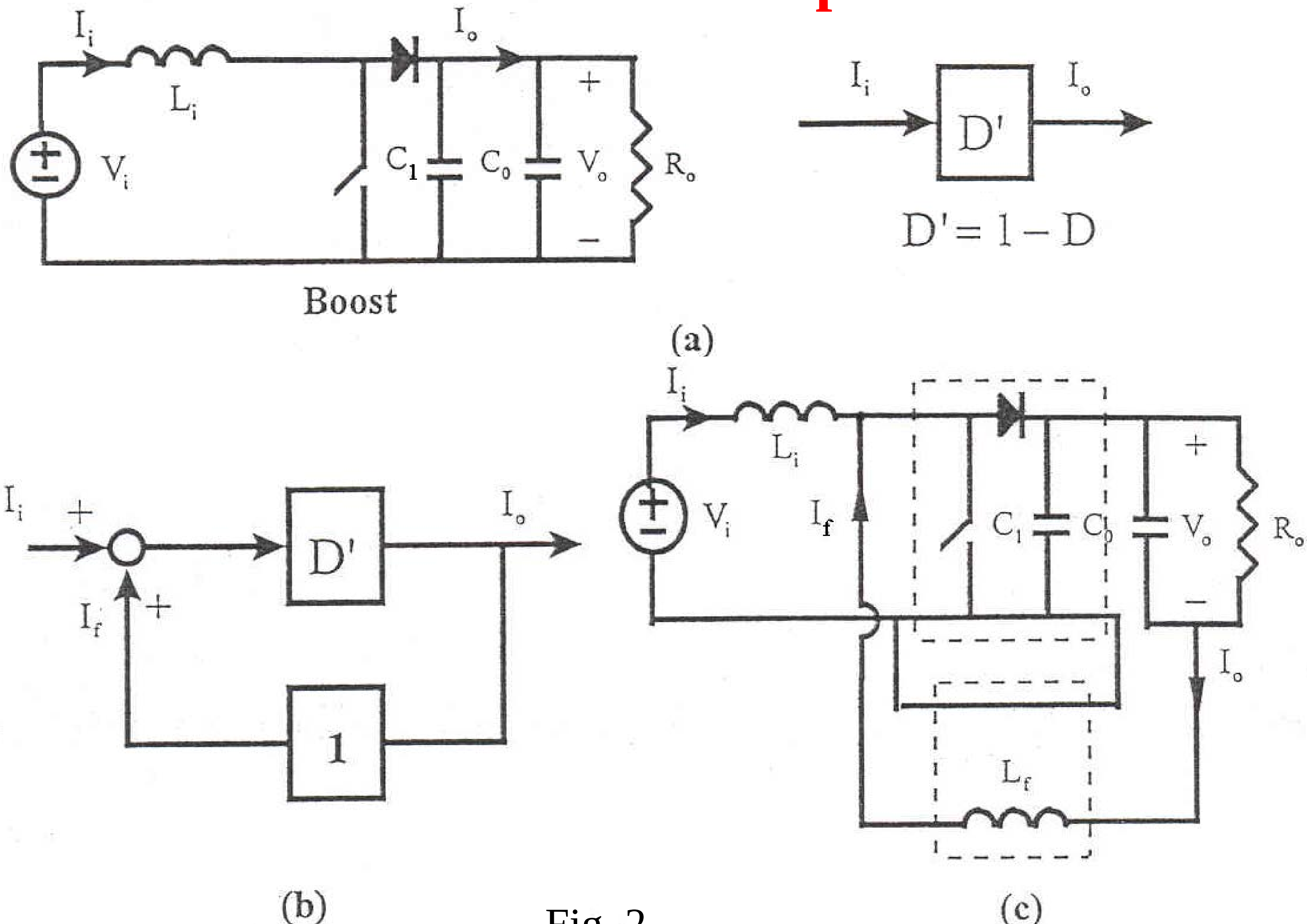
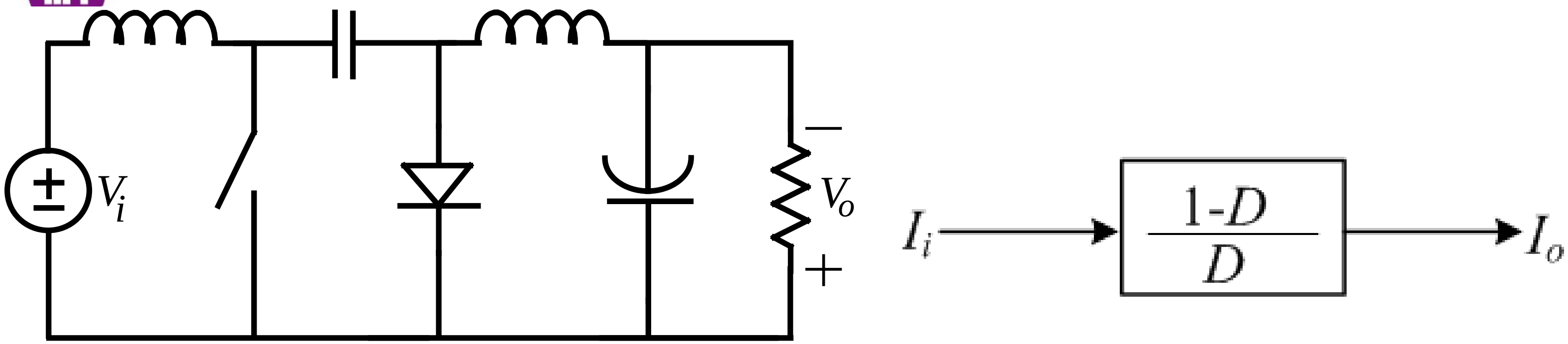
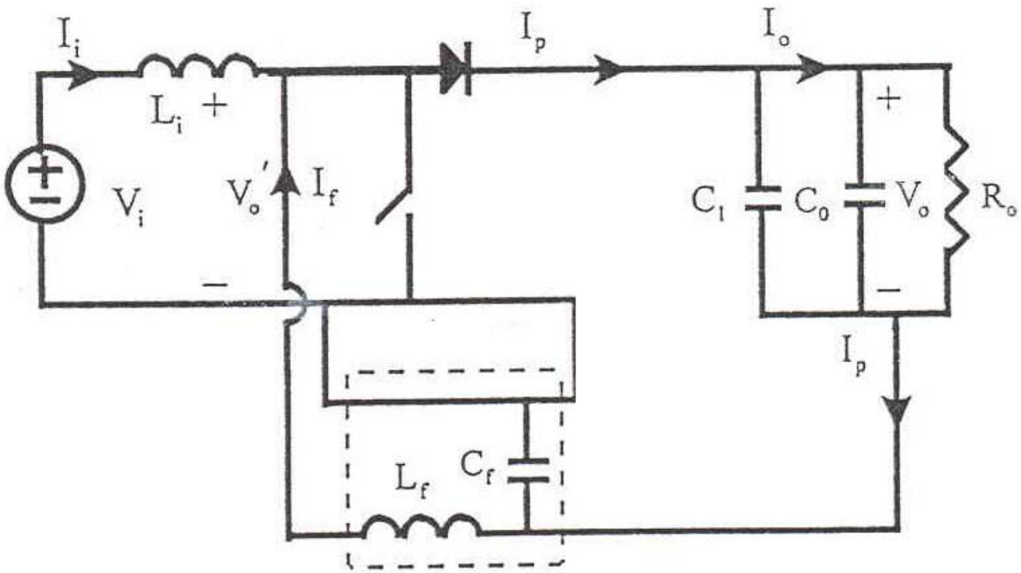


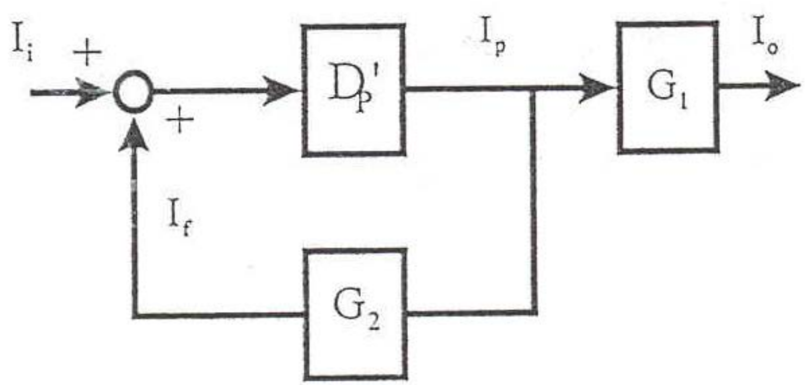
Fig. 2.



'Cuk Converter $\frac{V_o}{V_i} = \frac{D}{1-D}$ (d)



(e)



(f)

Fig. 2. (continued)

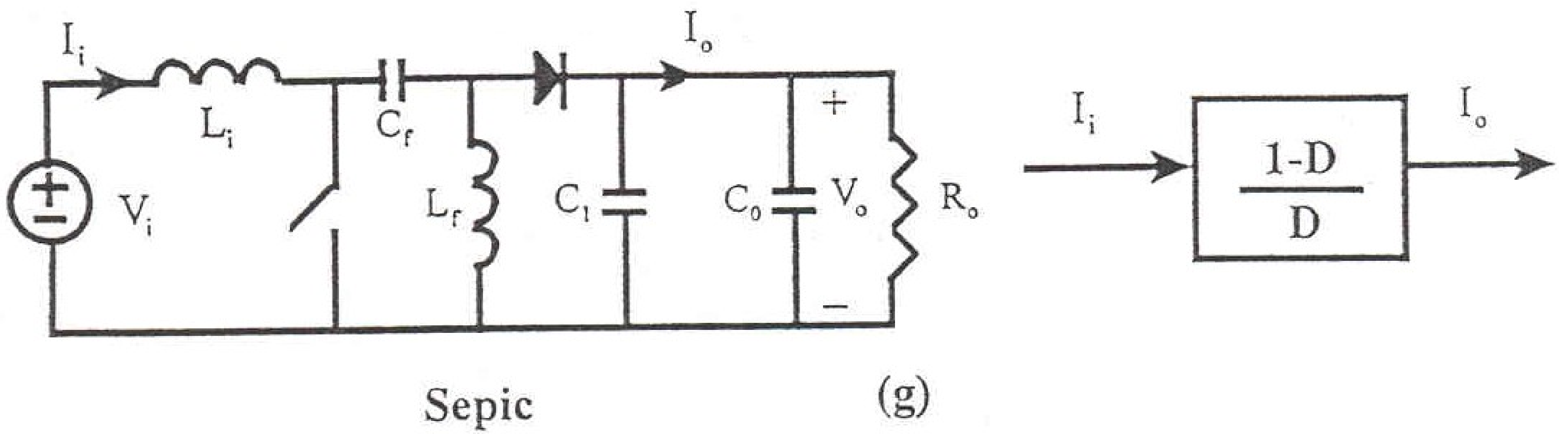


Fig. 2. (continued)

$$\frac{I_o}{I_i} = \frac{D_p^{'} G_1}{1 - D_p^{'} G_2}$$

Let $G_1 = G_2$,

at dc,

$$\frac{I_o}{I_i} = \frac{D^{'}}{1 - D^{'}} = \frac{1 - D}{D} .$$

By power conservation,

$$V_i I_i = V_o I_o ,$$

we have

$$\frac{V_o}{V_i} = \frac{D}{1 - D} .$$

Universal forms of buck-family and boost-family Converters

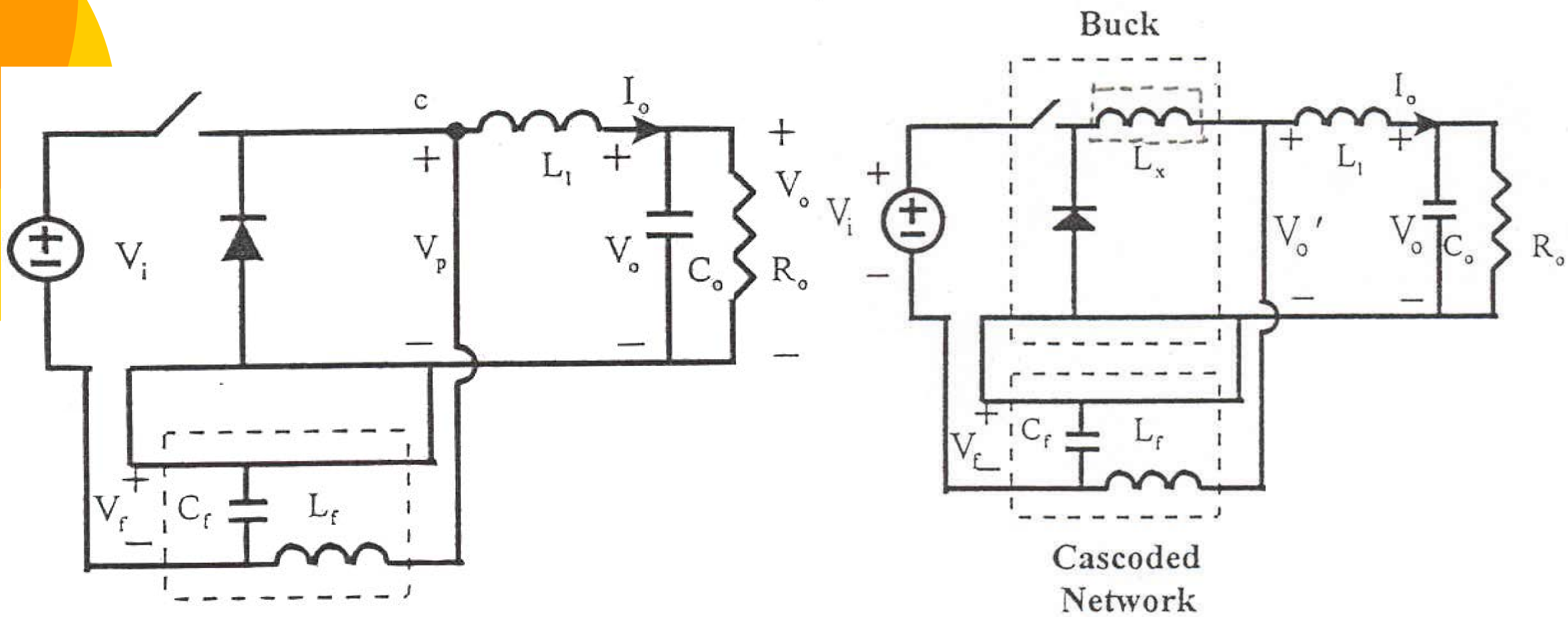
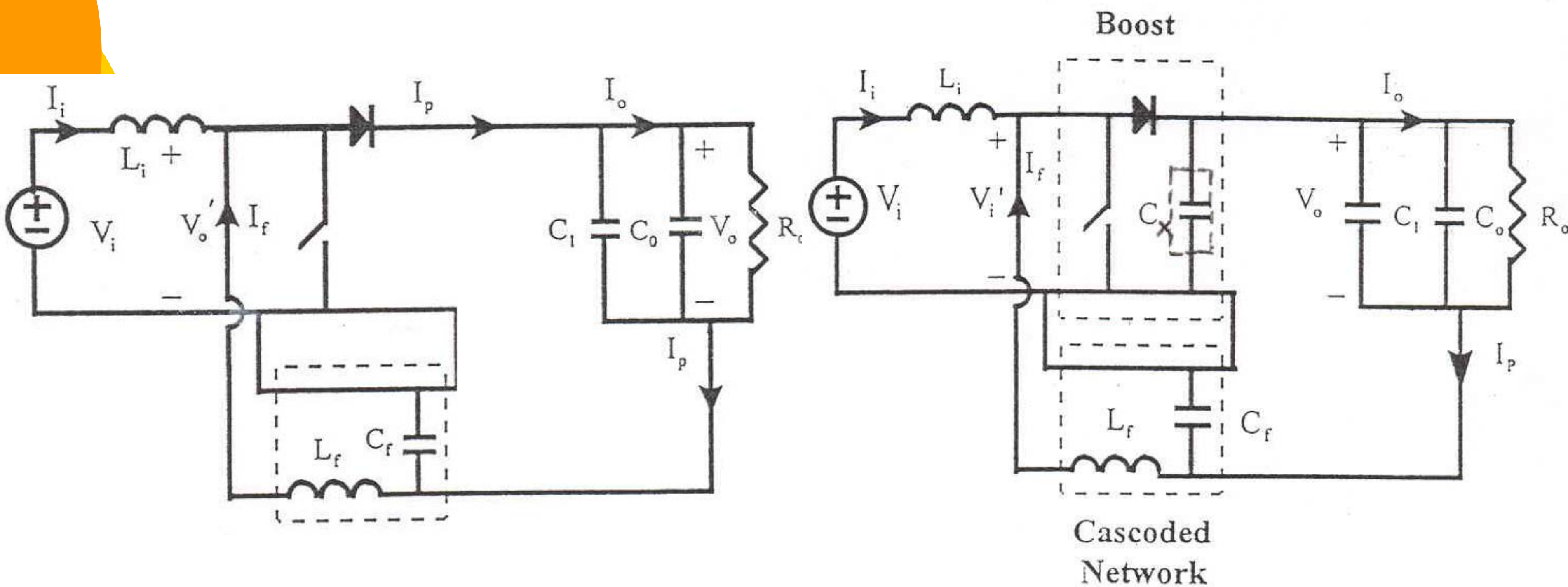


Fig. 3.



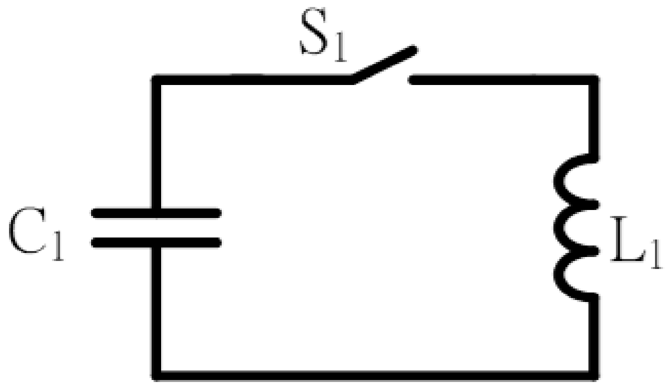
(b)

Fig. 3 (continued).

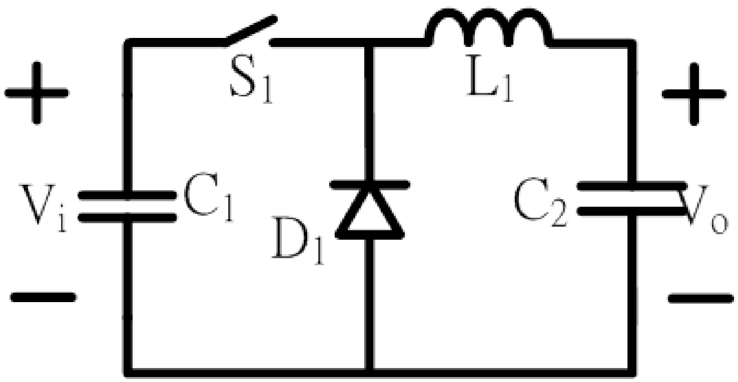
VI. Decoding and Synthesizing PWM Converters

- **Some Fundamentals**

A. Original Converter

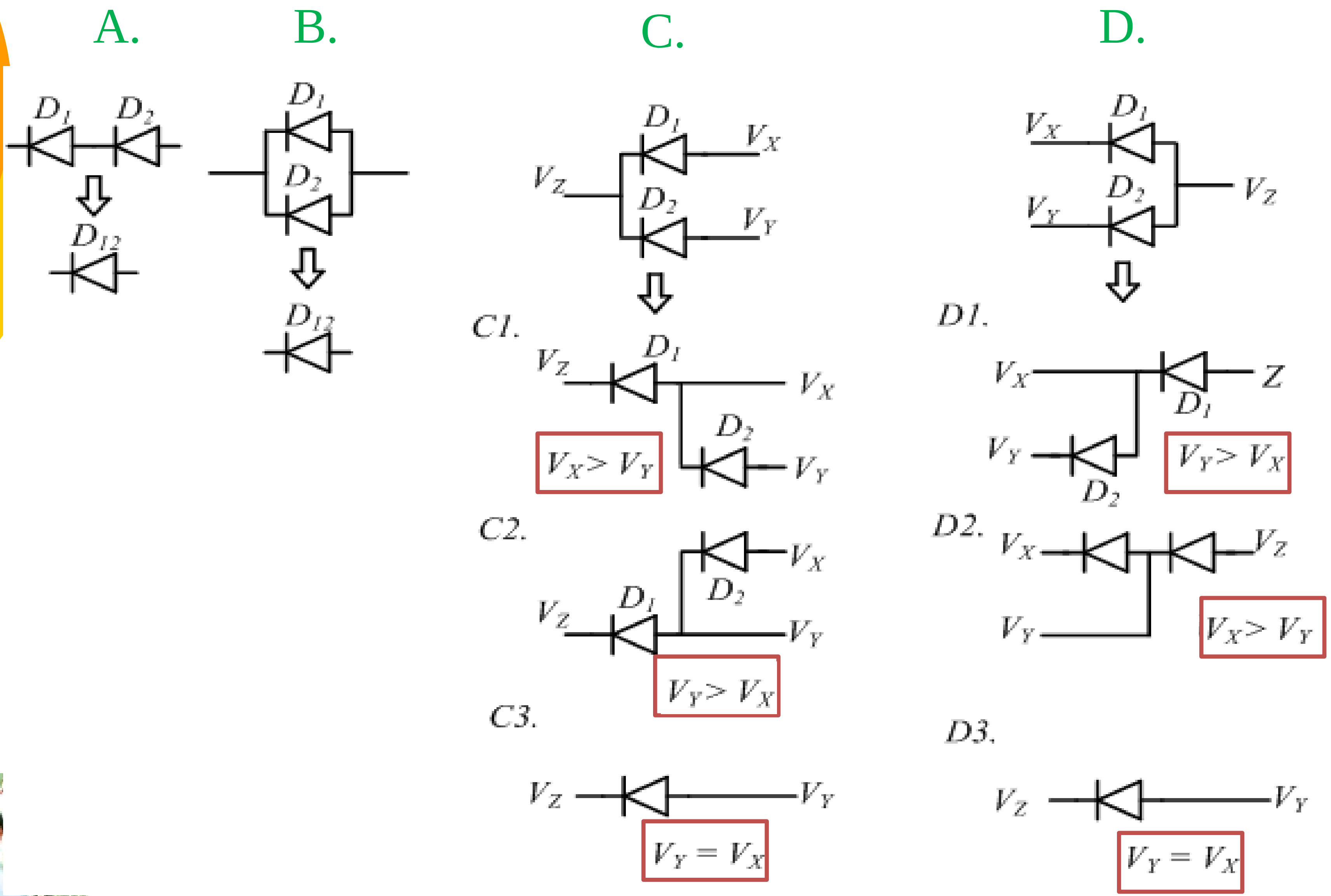


(a)



(b)

B. Diode Degeneration



C. DC Voltage/Current Offsetting

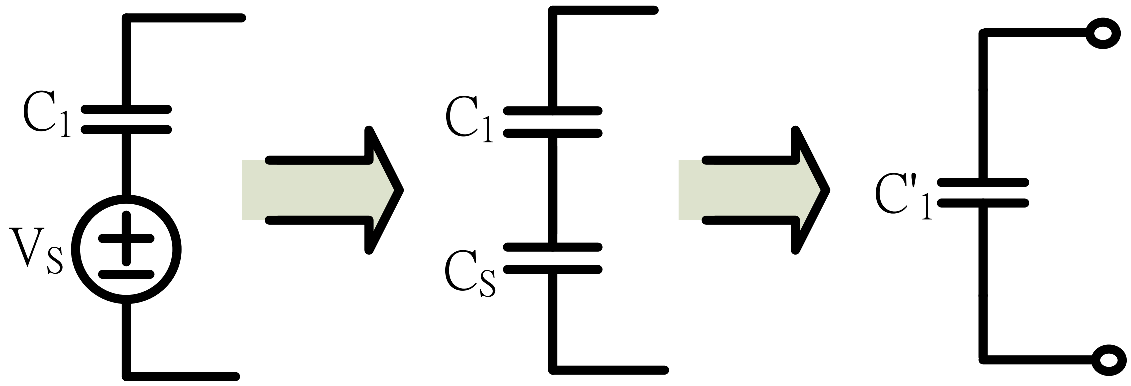


Fig. 4. A voltage source in series with a capacitor is equivalent to a single capacitor with a dc-offset voltage.

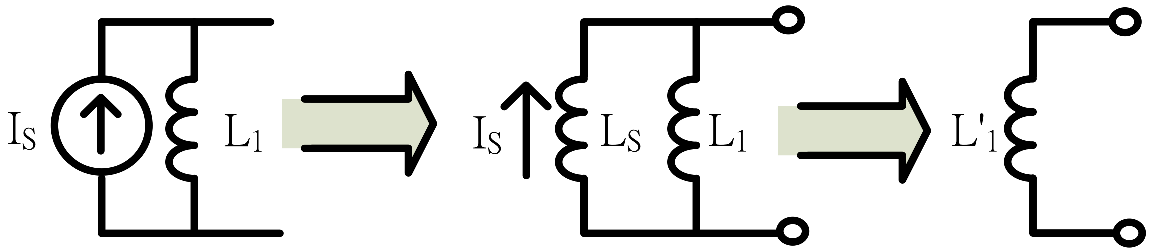
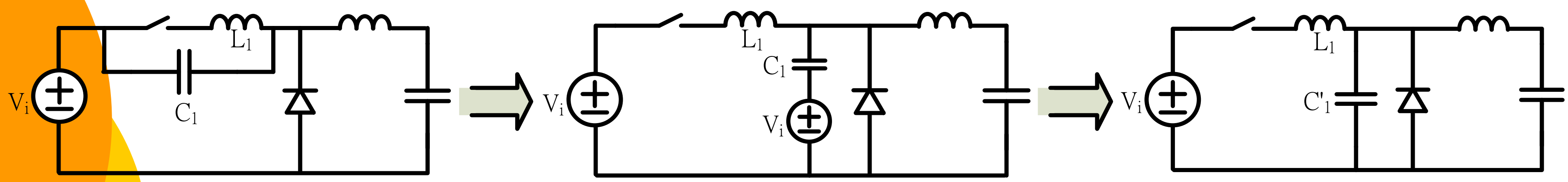
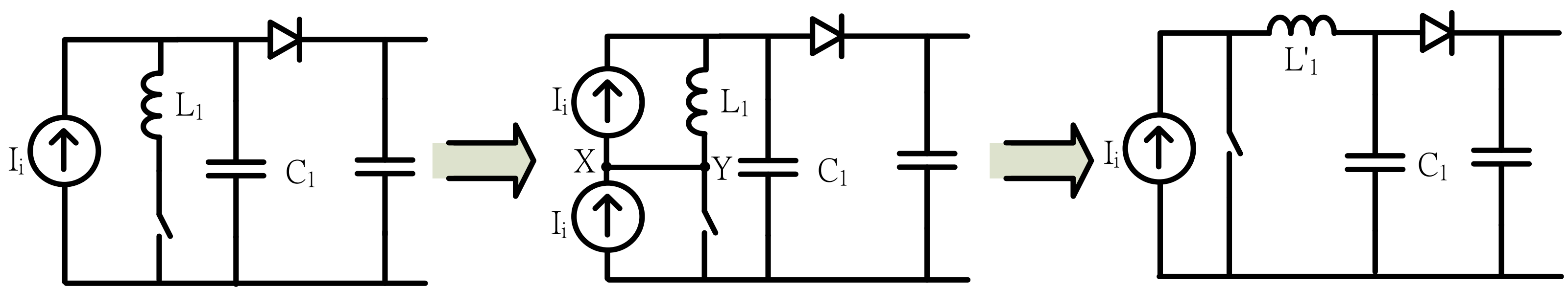


Fig. 5. A current source in parallel with an inductor is equivalent to a single inductor with a dc-offset current.



(a) (b) (c)

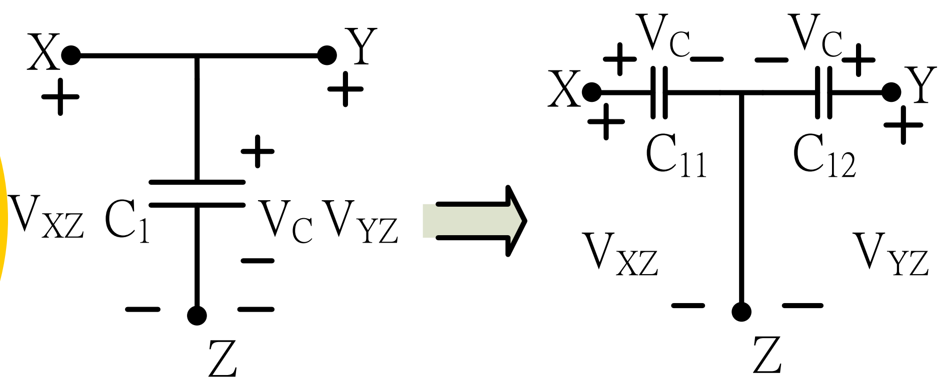
Fig. 6. Illustration of capacitor C_1 with different dc-offset voltages in a quasi-resonant buck converter.



(a) (b) (c)

Fig. 7. Illustration of inductor L_1 with different dc-offset currents in a quasi-resonant boost converter.

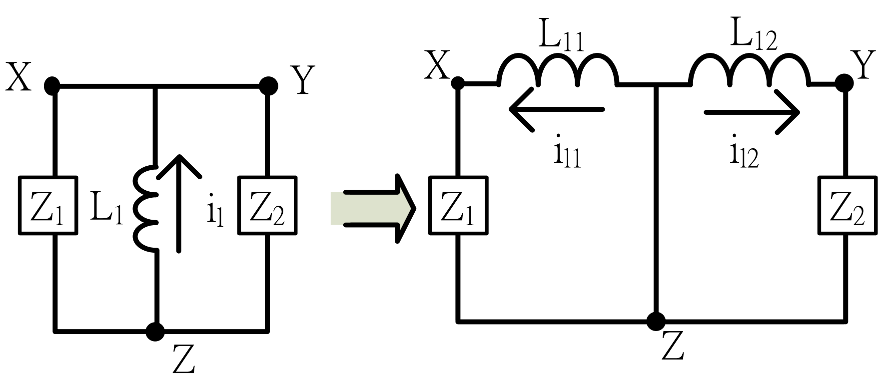
D. Capacitor/Inductor Component Splitting



a) $V_{XY} = 0$

b) $V_{XZ} = V_{YZ} = V_C$

Fig. 8. A capacitor is split into two capacitors with identical node voltages.



a) $i_{l1} + i_{l2} = i_l$.

b) In a valid converter topology, inductors L_{11} and L_{12} must be operated with volt-second balance in the steady state. Thus, their average voltage over a switching cycle will be zero, and $V_{XY} = 0$.

Fig. 9. An inductor is split into two inductors with identical total current and node voltages.

Three Fundamental PWM Converter

A. CCM Operation

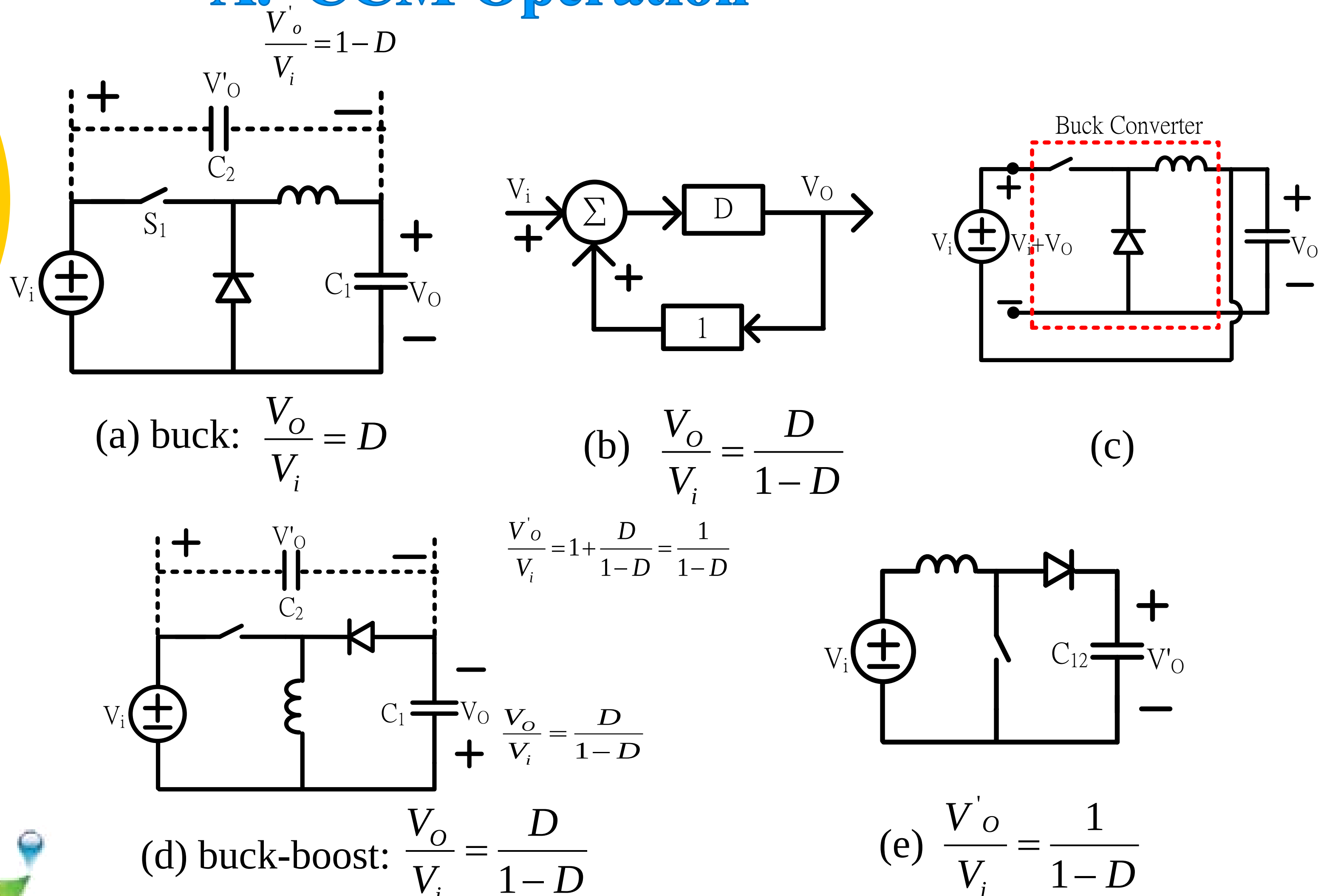


Fig. 10. Decoding and evolution of buck-boost and boost converters from the buck converter.

B. DCM Operation

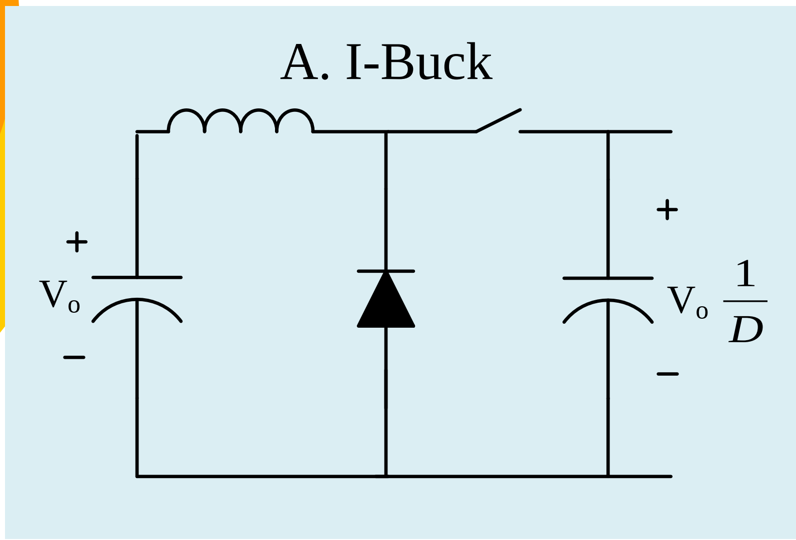
Buck : $\frac{d_1}{d_1+d_2}$ Boost : $\frac{d_1+d_2}{d_2}$

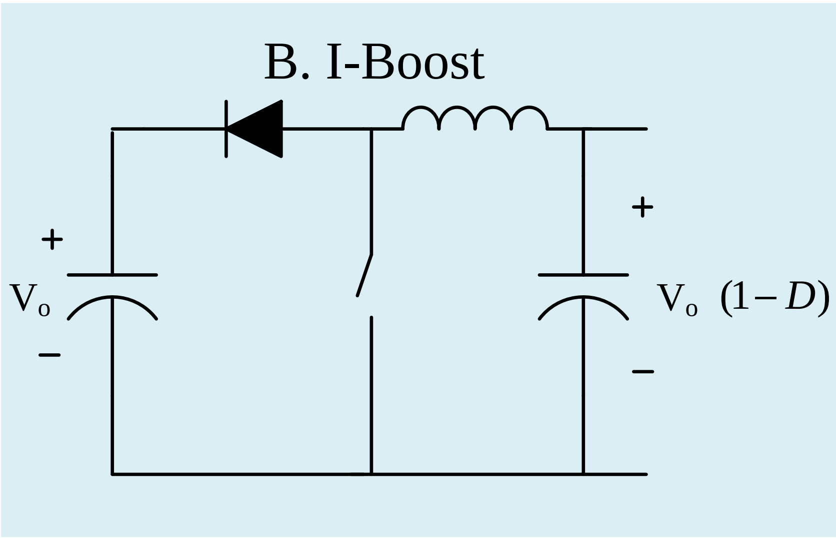
Buck-Boost : $\frac{d_1}{d_2}$

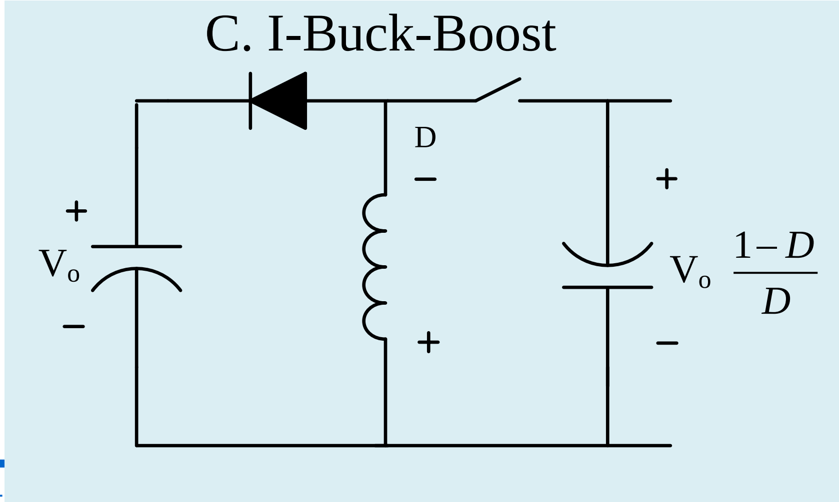
If $d_1 + d_2 = 1$, the operation mode will be CCM.

Thus, CCM is a special case of DCM operation.

• Inverse Buck, Boost and Buck-Boost







➢ Deduction from Ćuk, SEPIC and Zeta to Buck-Boost Converter (with DC Voltage Offsetting)

A. From Ćuk to Buck-Boost

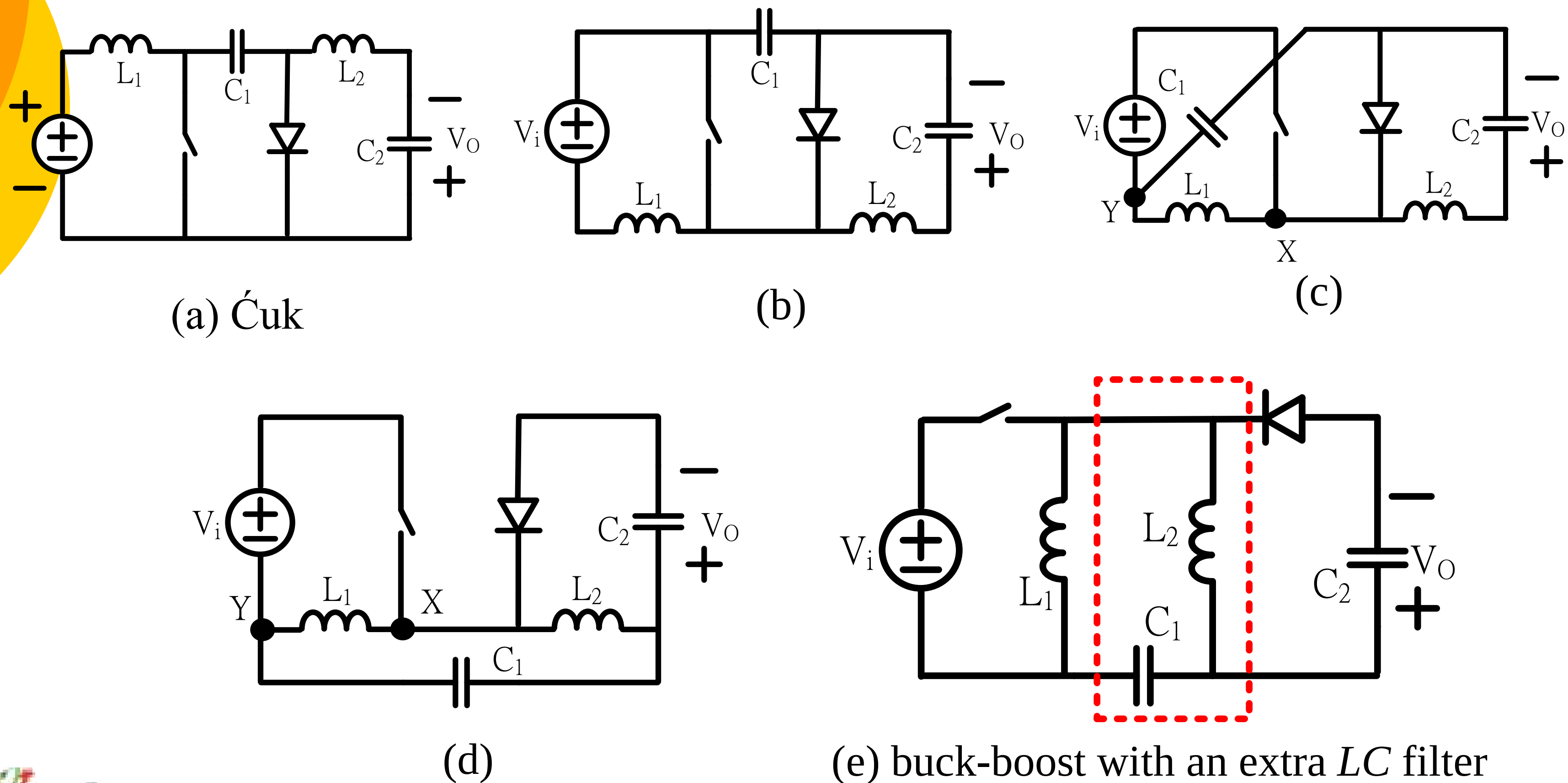


Fig. 11. Deduction from Ćuk to buck-boost converter.

B. From SEPIC to Buck-Boost

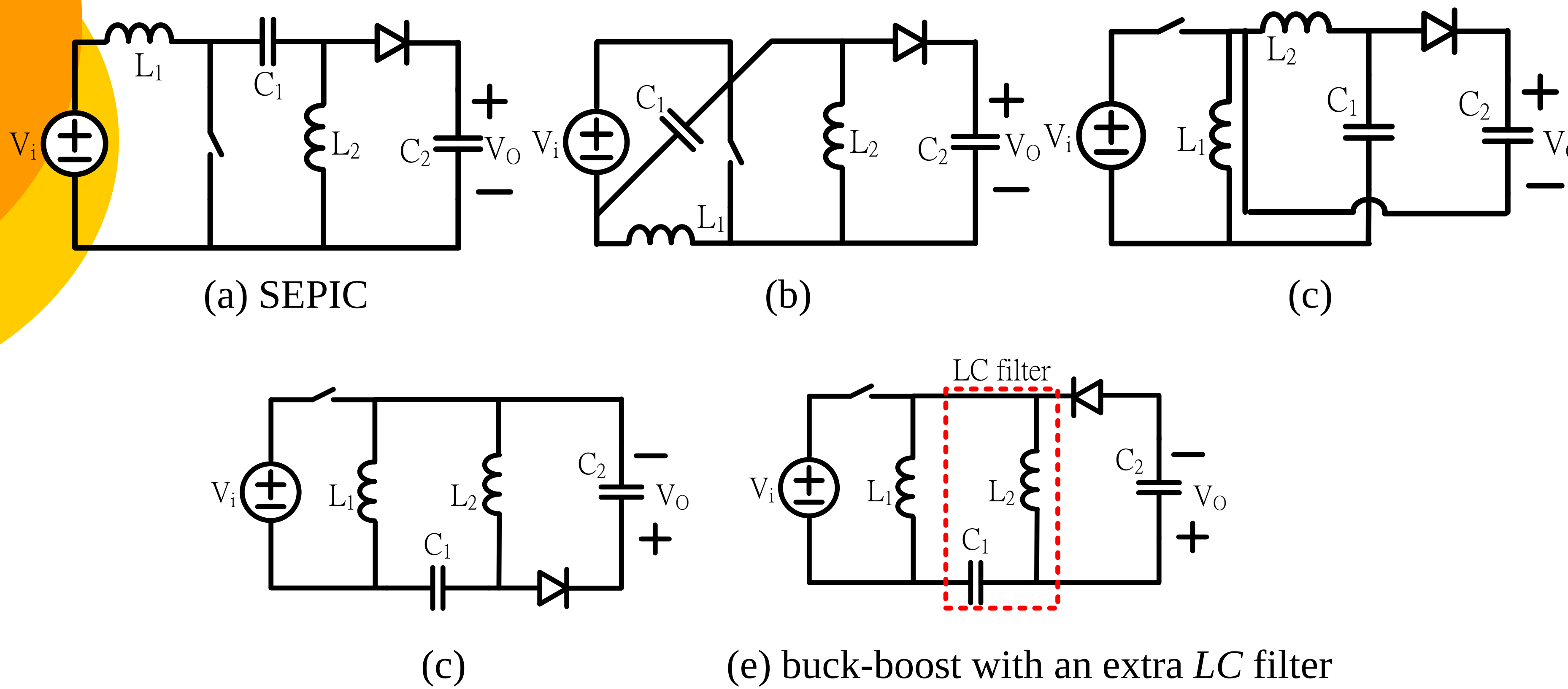


Fig. 12. Deduction from SEPIC to buck-boost converter

C. From Zeta to Buck-Boost

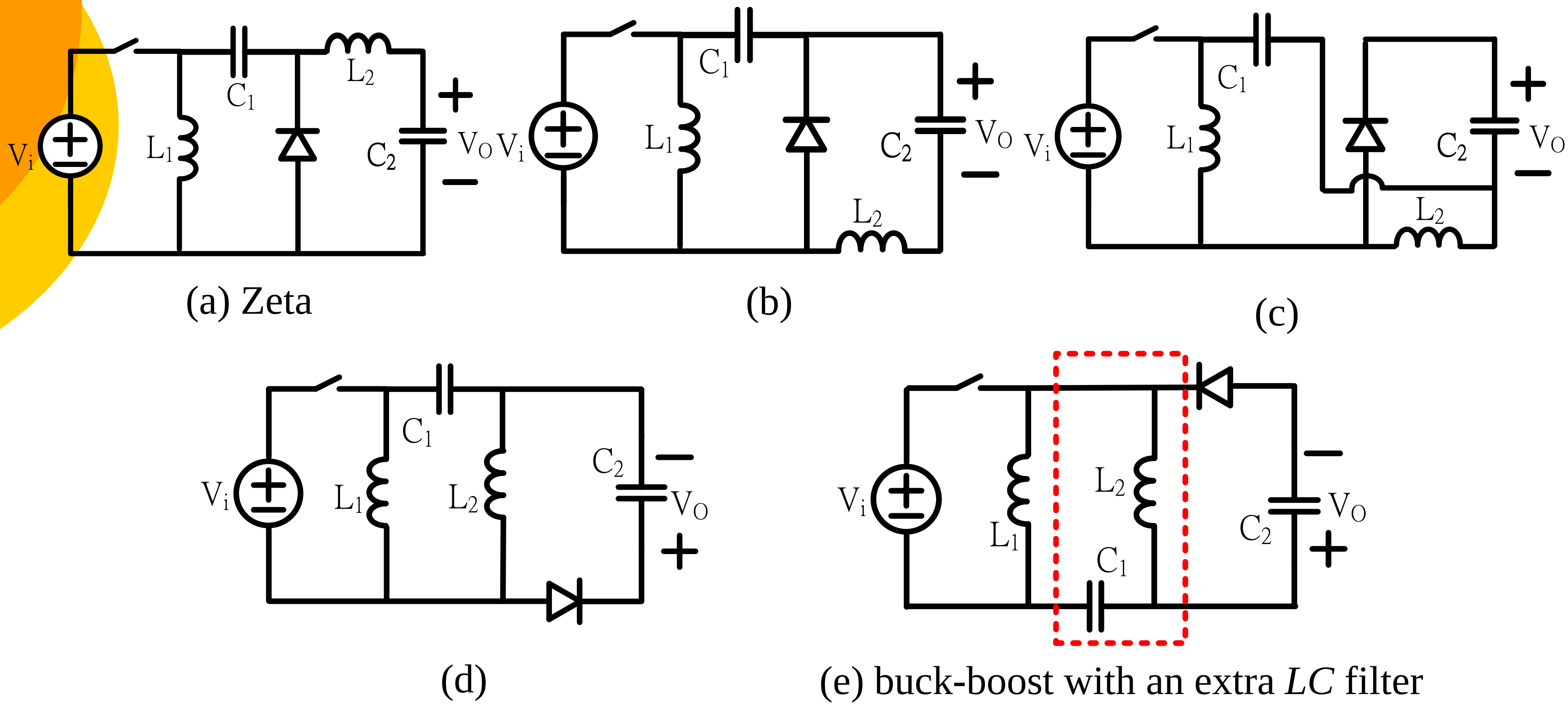


Fig. 13. Deduction from Zeta to buck-boost converter.

D. Deduction from SEPIC to Zeta and Ćuk

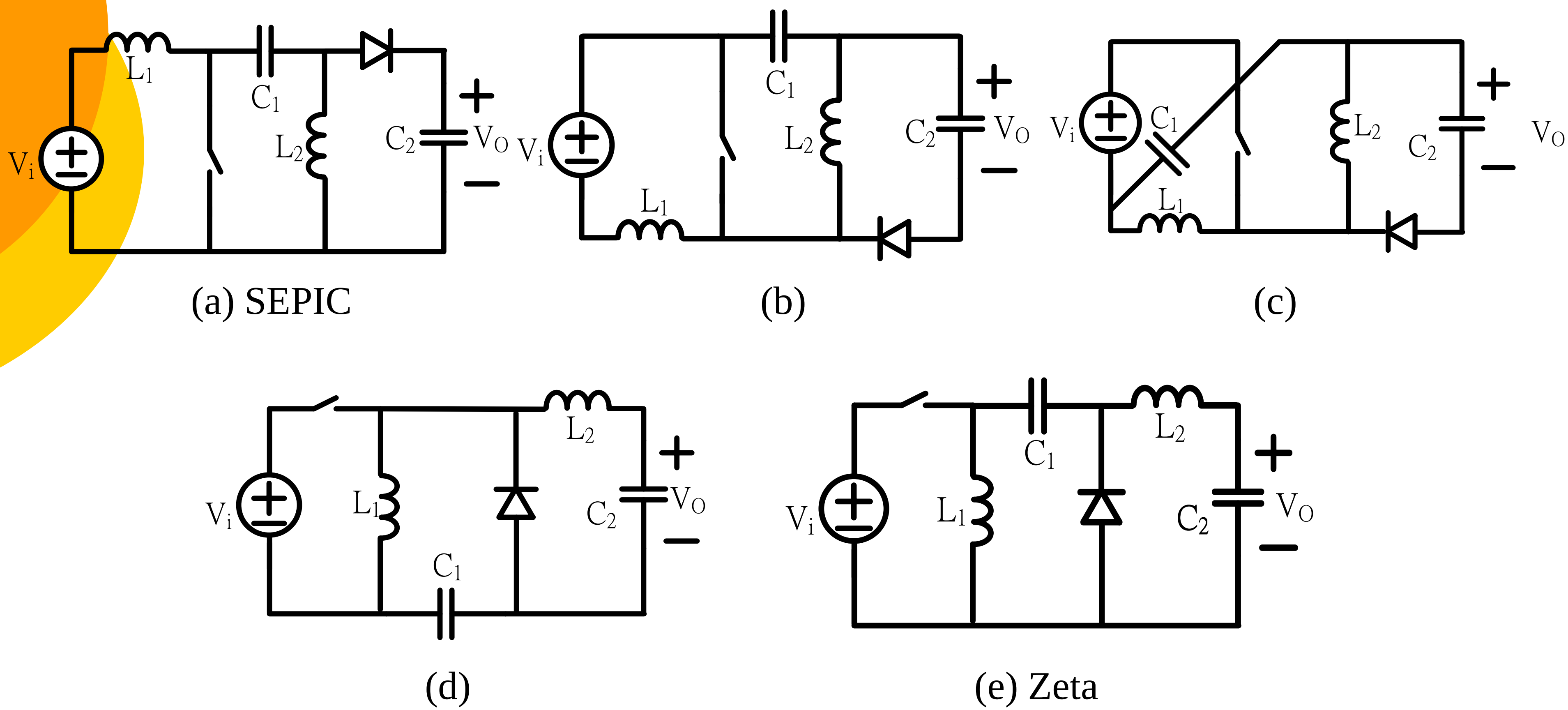


Fig. 14. Evolution of Zeta converter from SEPIC.

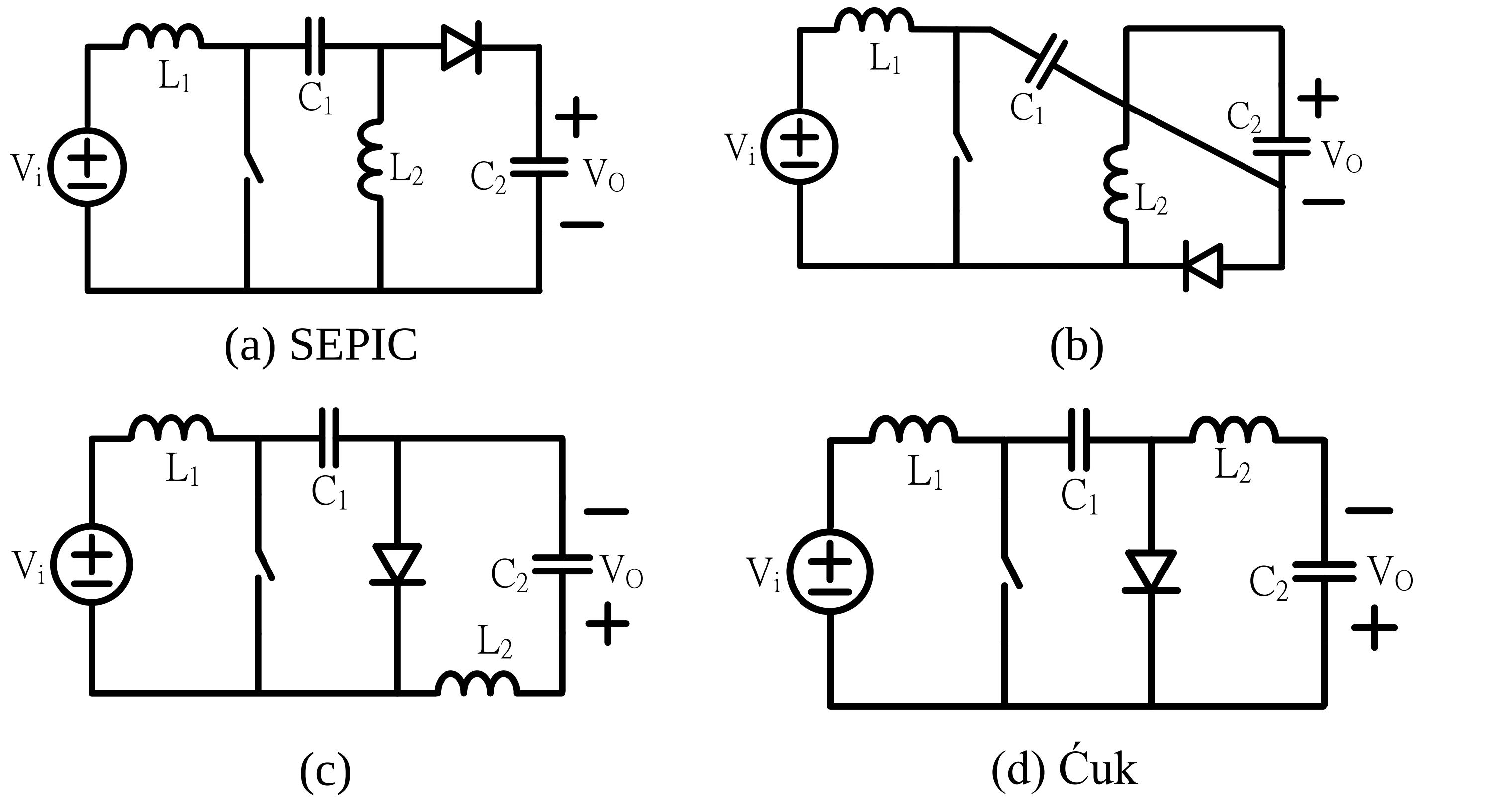


Fig. 15. Evolution of Ćuk converter from SEPIC

Processes of Decoding and Synthesizing

1) **Using a long division to detach the unity gain from a given transfer gain.**

Eg. $$f(D)=\frac{V_o}{V_i}=\frac{1-D}{1-2D}=1+\frac{D}{1-2D}=1+\frac{V'_o}{V_i}=1+f_r(D) \qquad (1)$$

2) **Conducting a cross multiplication of $V'_o/V_i = f_r(D)$ to find a relationship among V_i, V'_o and D:**

$$\frac{V'_o}{V_i}=f_r(D)=\frac{D}{1-2D} \quad \text{Or,} \quad V'_o(1-D)=(V_i+V'_o)D \qquad (2)$$

That is,

$$V'_o=(V_i+V'_o)\frac{D}{1-D} \qquad (3)$$

3) **Using a transfer block diagram to illustrate equation (3) and adding up with the unity gain if it exists.**

4) **Synthesizing the transfer block diagram with the original converter and its derived.**

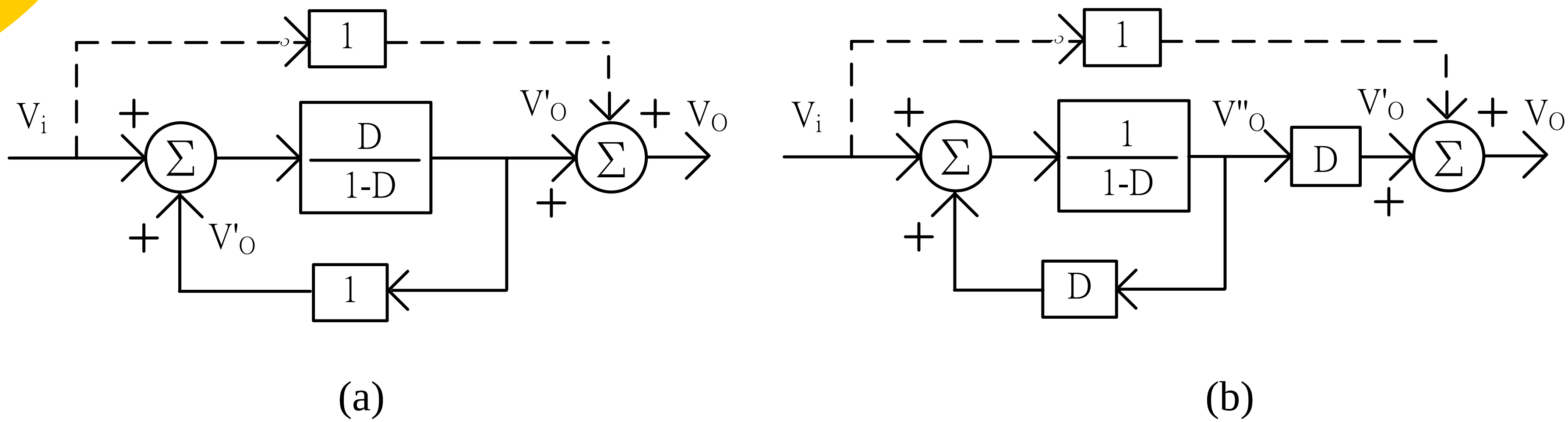


Fig. 10. Two transfer block diagrams to represent the transfer gain of $V_o/V_i = (1\text{-}D)/(1\text{-}2D)$.

➢ Decoding and Synthesizing PWM Converters

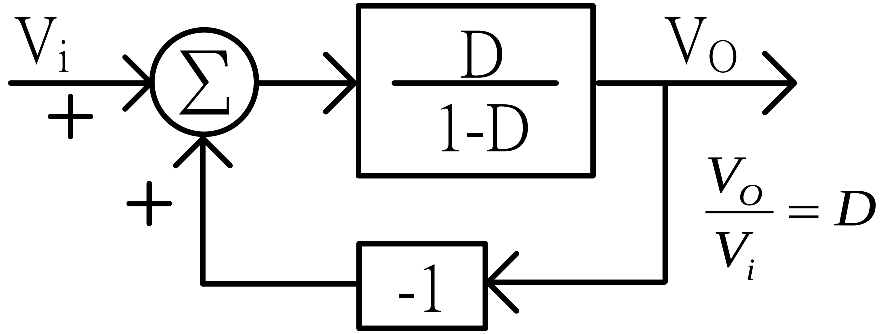


Fig. 16. A buck converter is decoded with *D/(1-D)* and a negative unity feedback.

1. Synthesizing with Buck-Boost

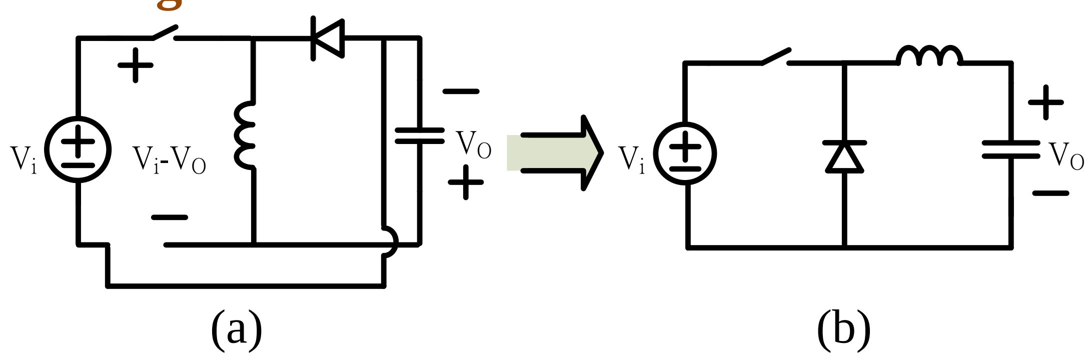


Fig. 17. Derivation of the buck converter from the decoded form shown in Fig. 16 and the buck-boost converter.

2. Synthesizing with Ćuk

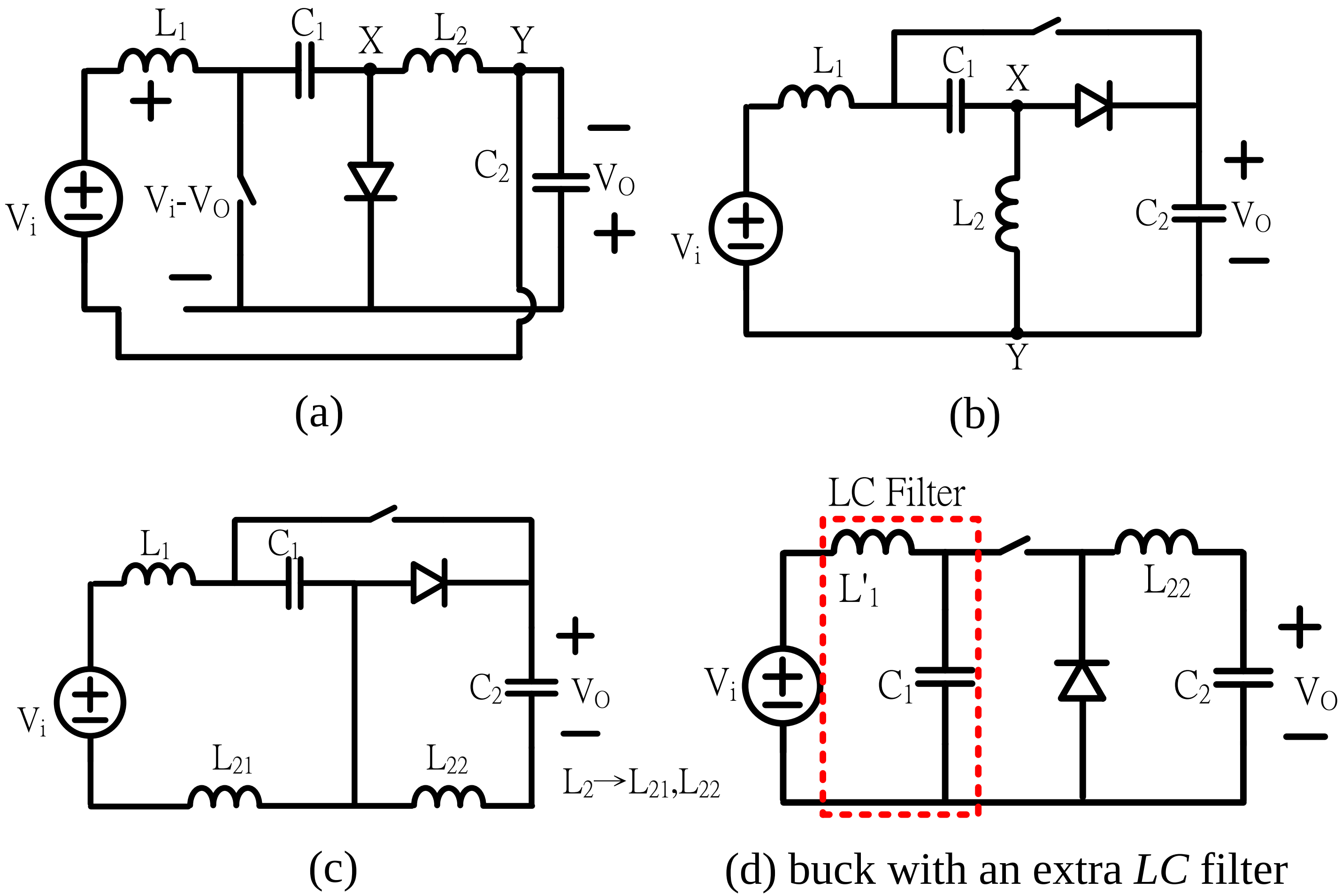
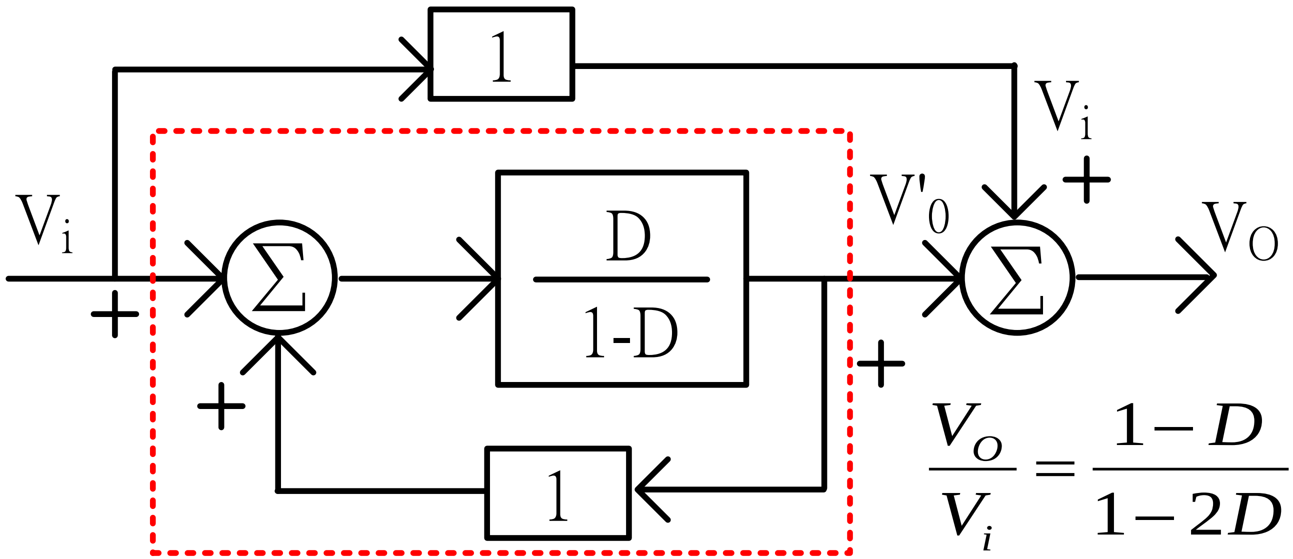


Fig. 18. Derivation of buck converter from the decoded form shown in Fig. 16 and the Ćuk converter.

A. Voltage-Fed Z-Source Converter

- **Decoding (1-D)/(1-2D)**



$$\frac{V_O}{V_i} = \frac{1-D}{1-2D}$$

Fig. 19. A transfer block diagram to decode $V_o/V_i = (1\text{-}D)/(1\text{-}2D)$

• **Synthesizing with SEPIC**

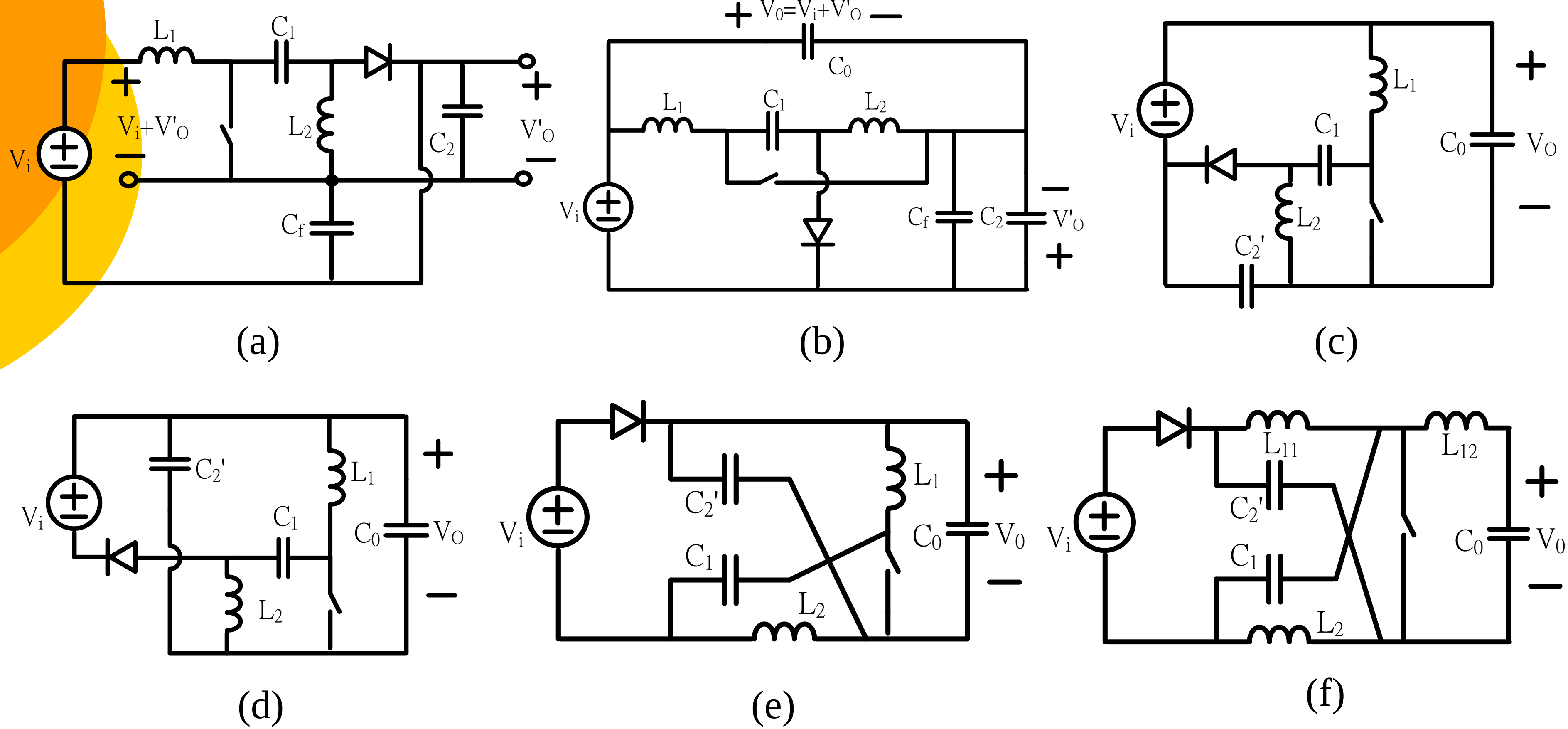


Fig. 20. Synthesizing the transfer block diagram shown in Fig. 19 with the SEPIC converter.

- **Synthesizing with Zeta**

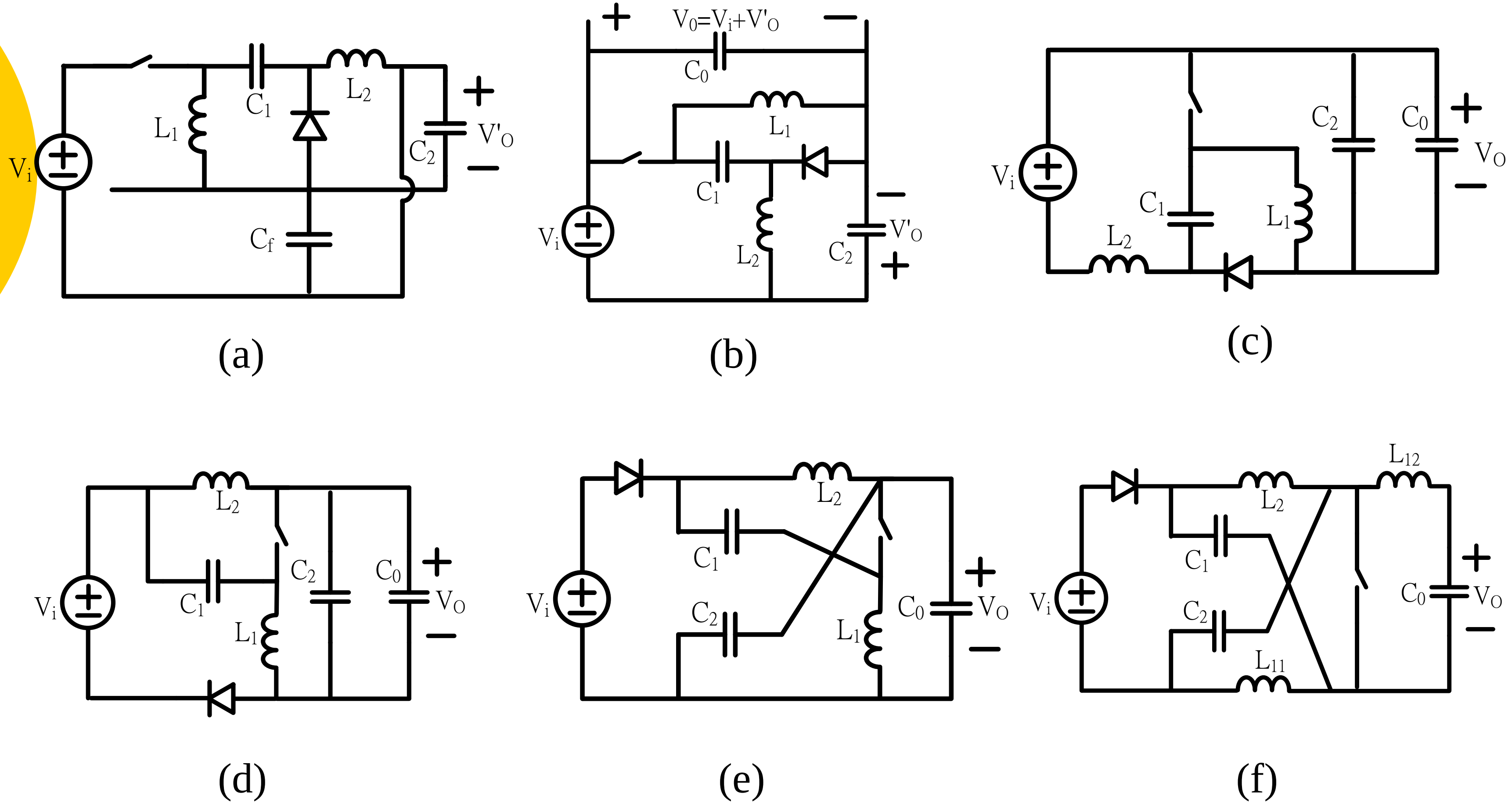


Fig. 21. Synthesizing the transfer block diagram shown in Fig. 19 with the Zeta converter

B. Current-Fed Z-Source Converter

- Synthesizing with SEPIC

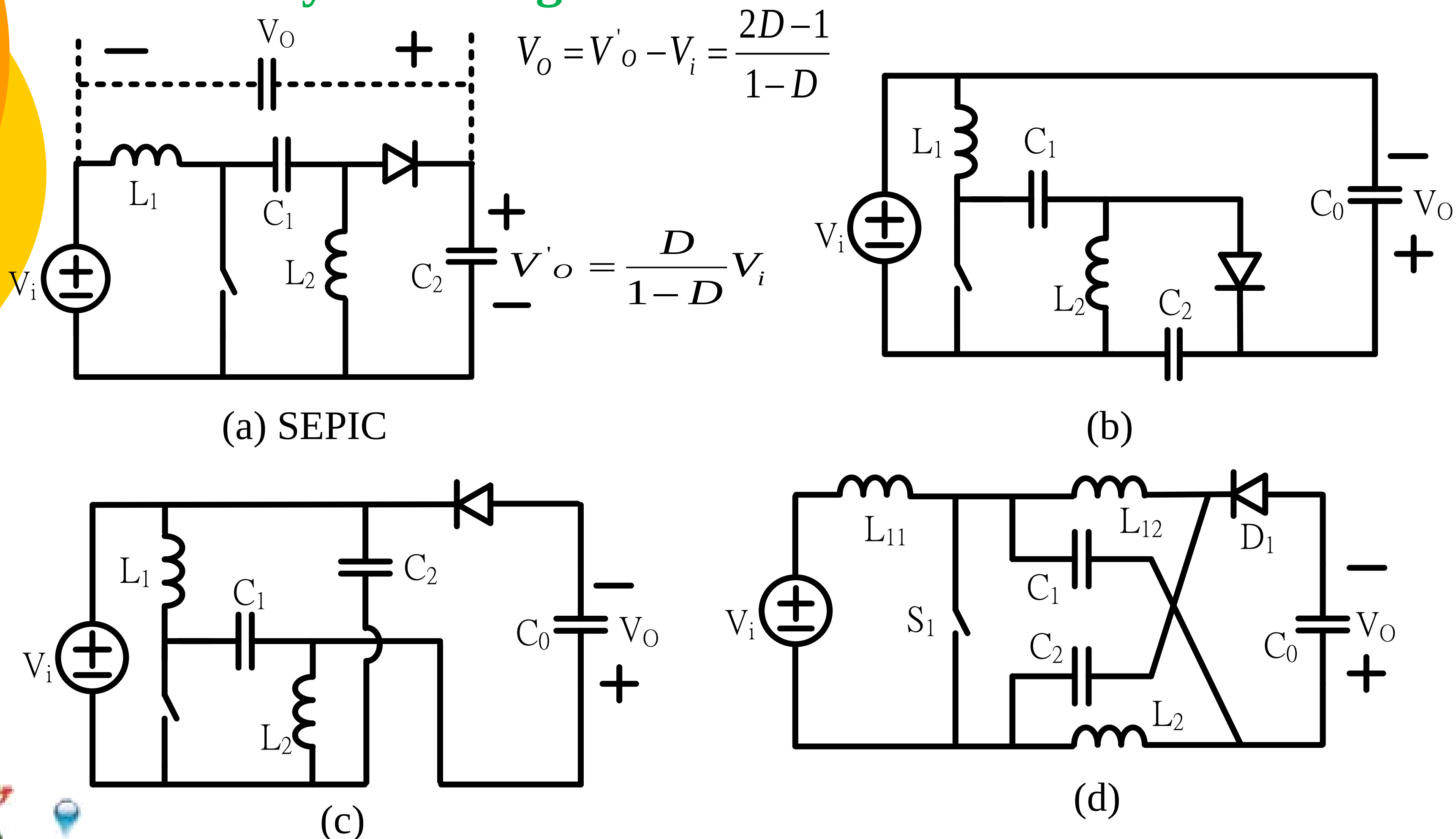


Fig. 22. Synthesizing the transfer gain $V_O/V_i = (2D-1)/(1-D)$ with a SEPIC converter

- **Synthesizing with Zeta**

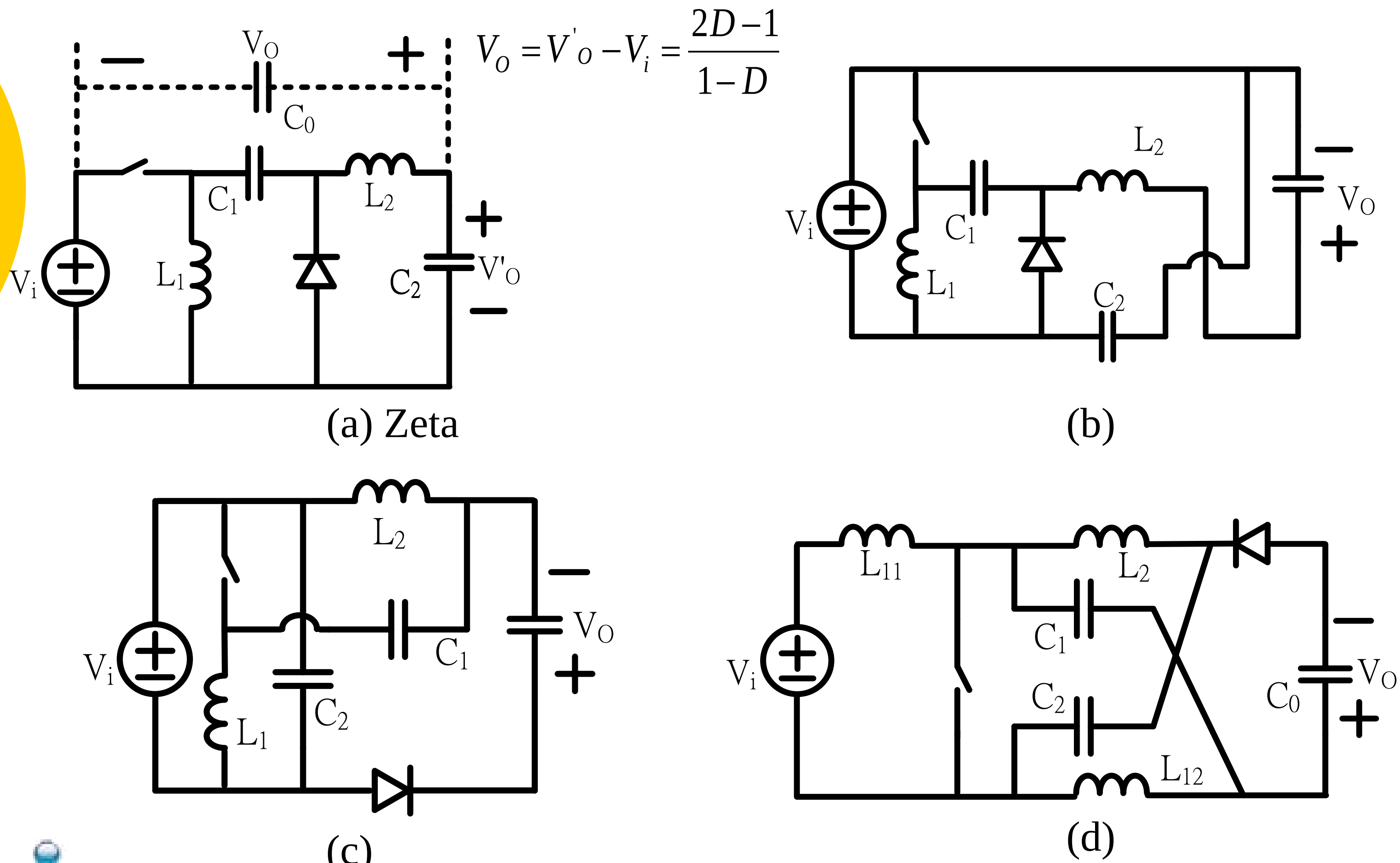


Fig. 23. Synthesizing the transfer gain $V_O/V_i = (2D-1)/(1-D)$ with a Zeta converter

C. Quasi Z-Source Converter

- **Decoding** **D/(1-2D)**

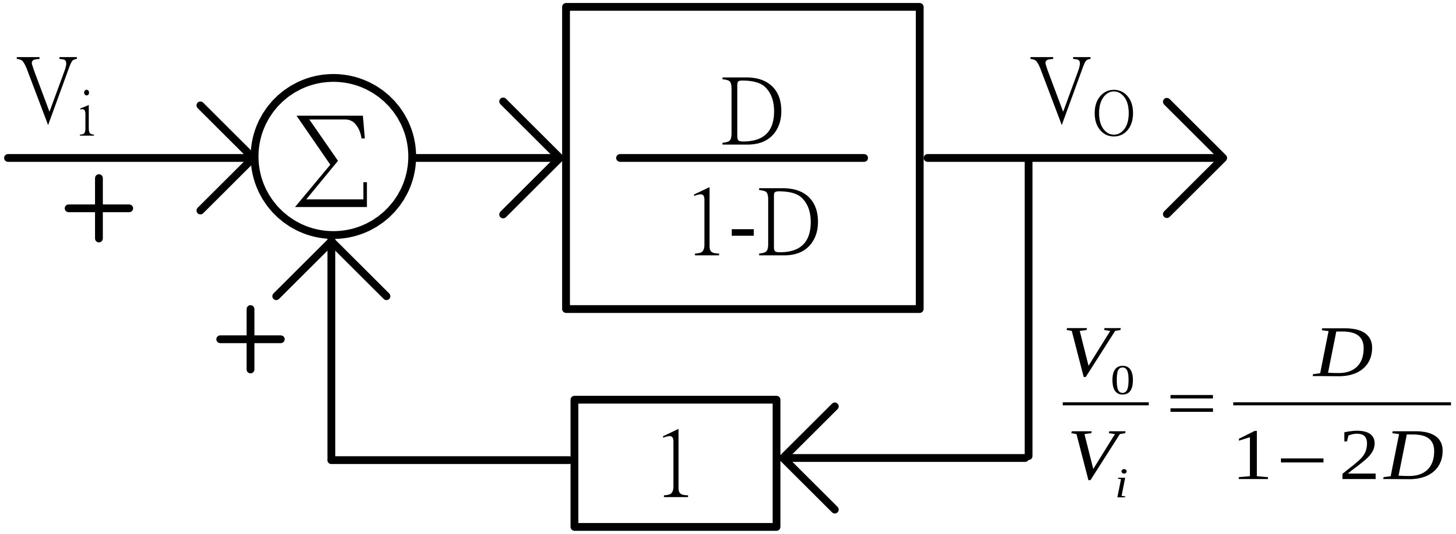


Fig. 24. A transfer gain block of *D/(1-D)* with a positive unity feedback yielding $V_O/V_i = D/(1-2D)$

• Synthesizing with **SEPIC**

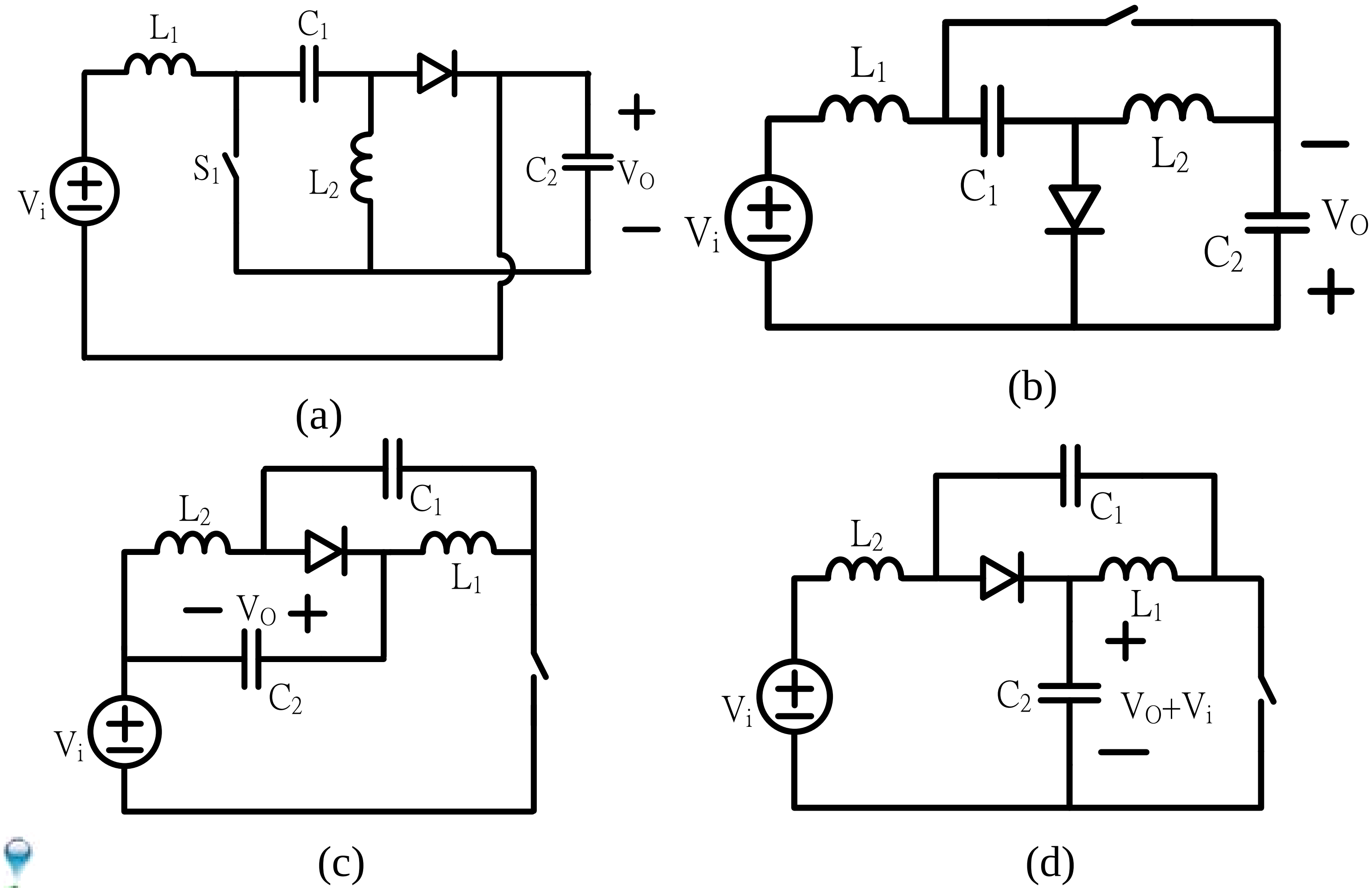


Fig. 25. Synthesizing $V_O/V_i = D/(1\text{-}2D)$ with a SEPIC converter

• Synthesizing with Zeta

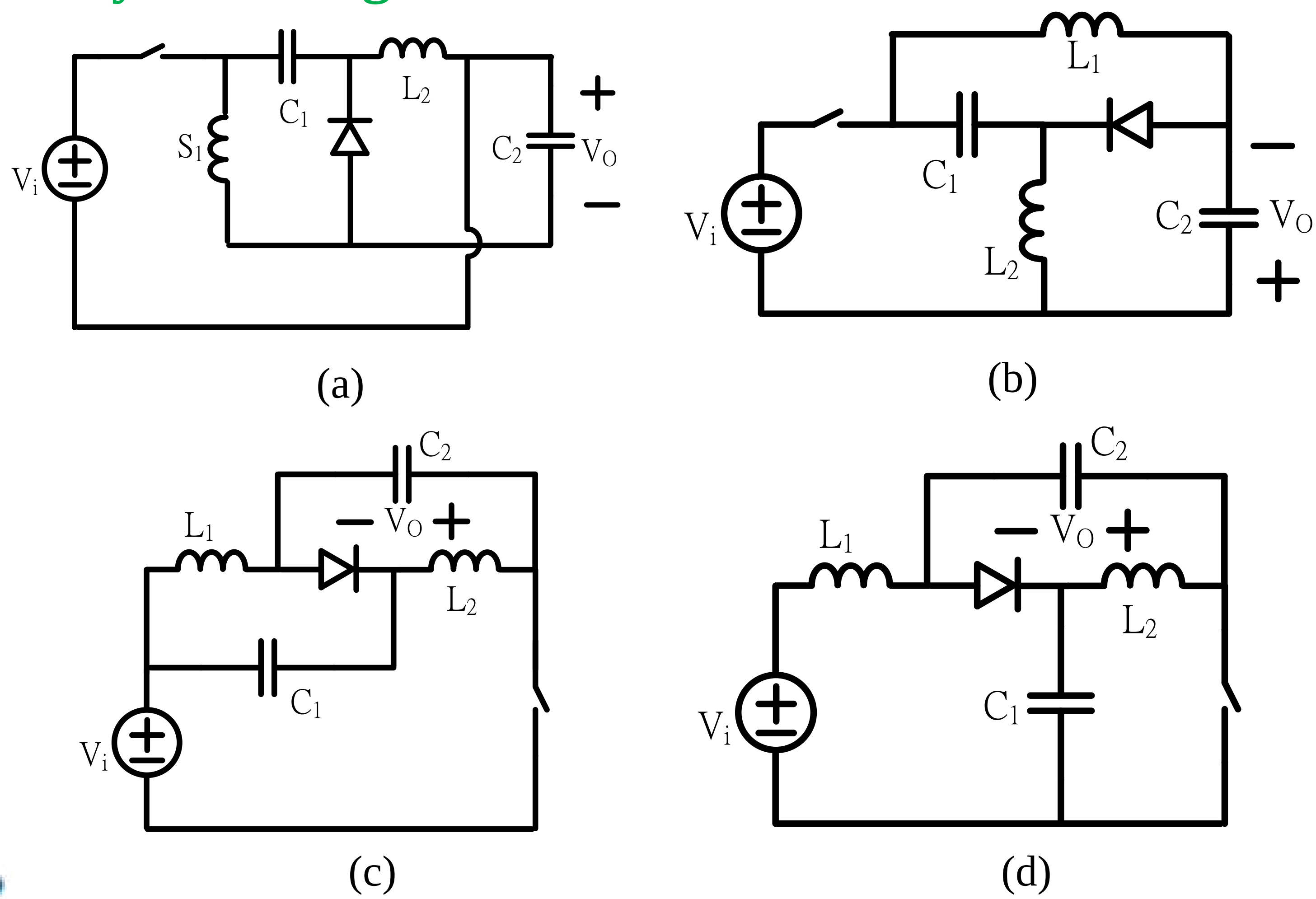
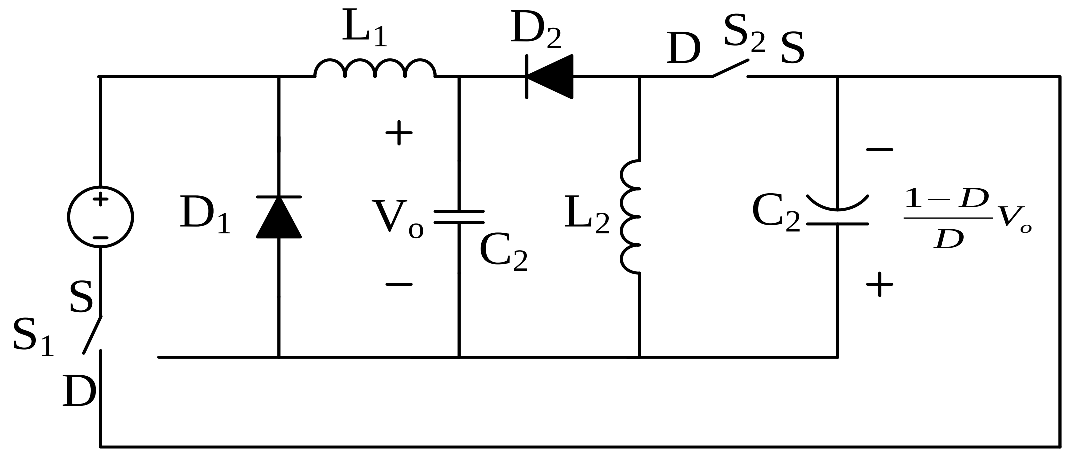


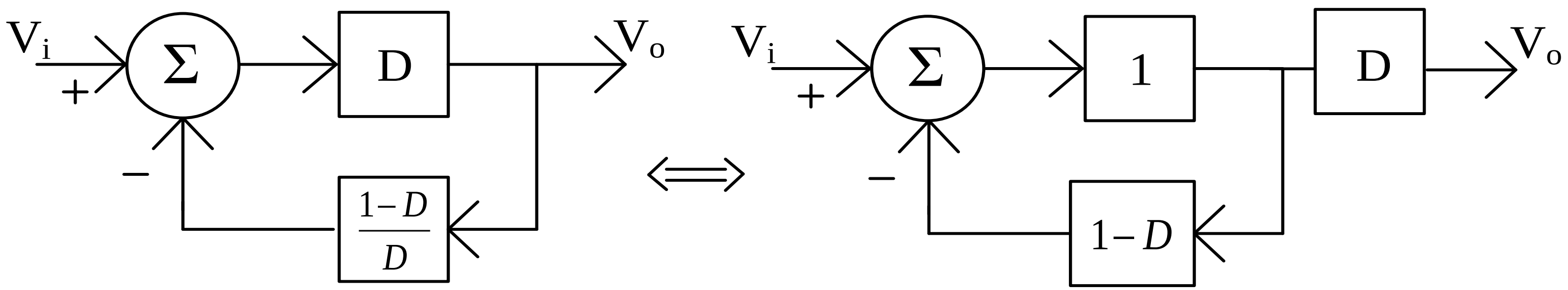
Fig. 26. Synthesizing $V_O/V_i = D/(1\text{-}2D)$ with a Zeta converter

Decoding D/(2-D)

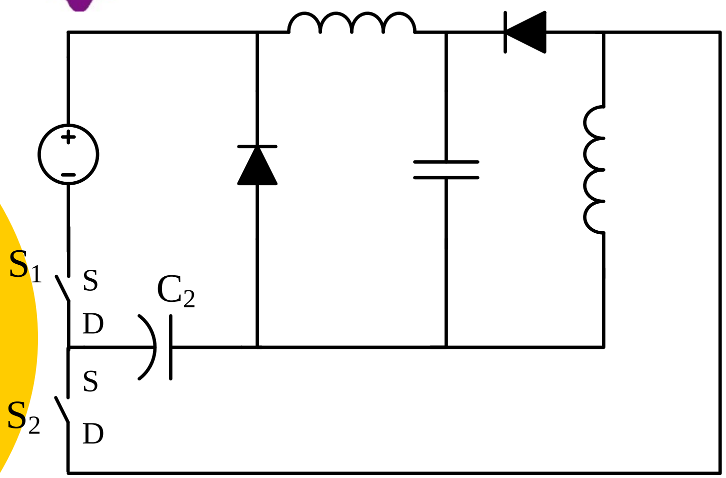
1. Synthesizing with Buck +I-Buck-Boost



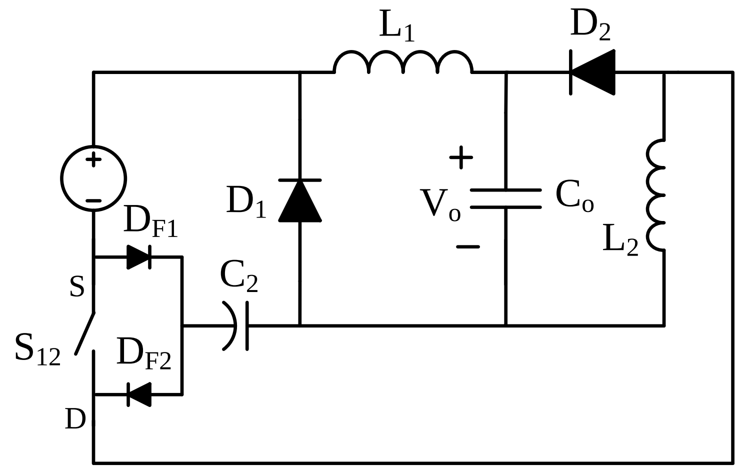
(a)



$$\frac{V_o}{V_i} = \frac{D}{2-D}$$

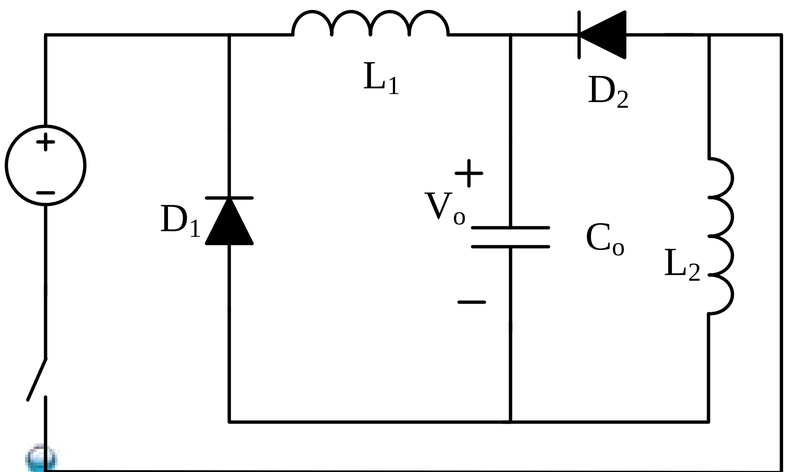


(b)

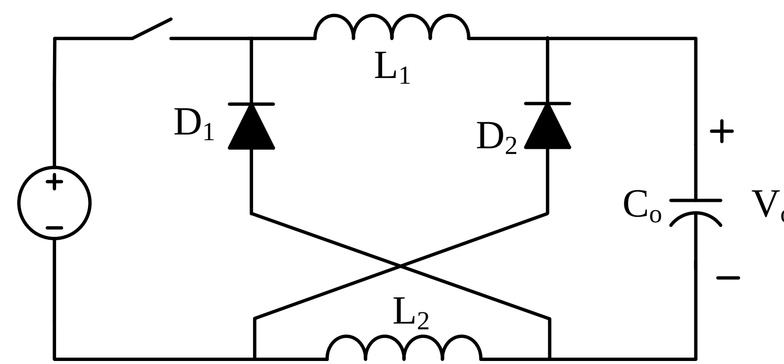


$I_1 = I_2 \rightarrow D_{F1}$ and D_{F2} can be saved (open)

(c)

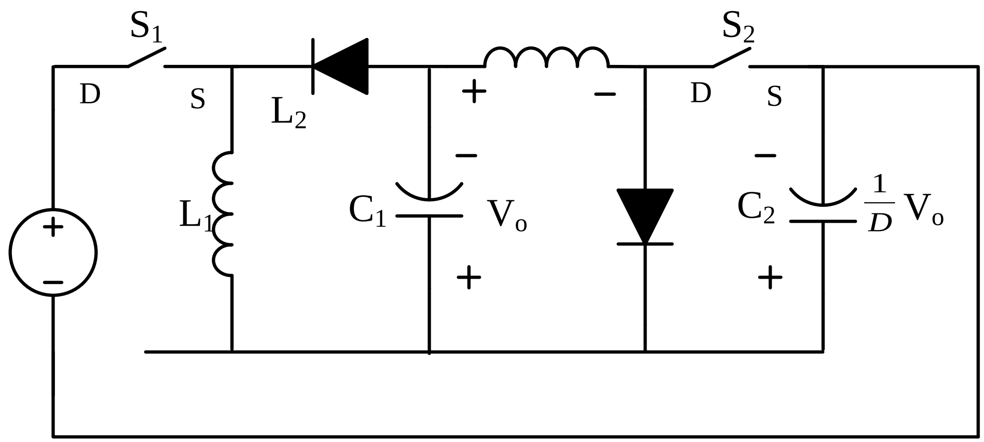


(d)

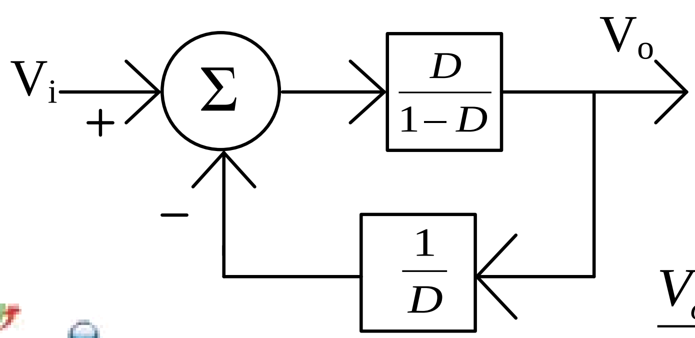


(e) [48]

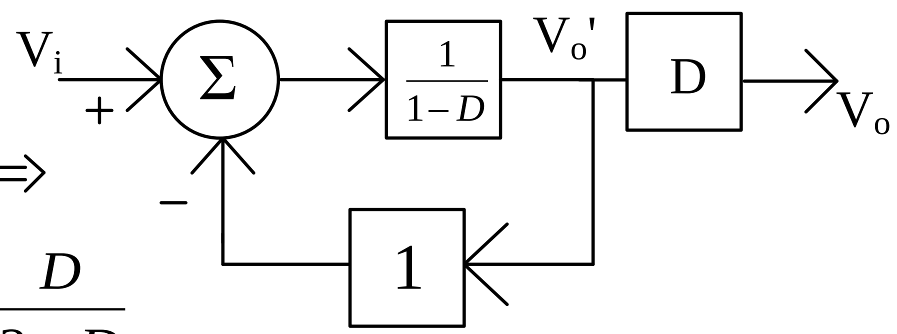
2. Synthesizing with Buck-Boost + I-Buck



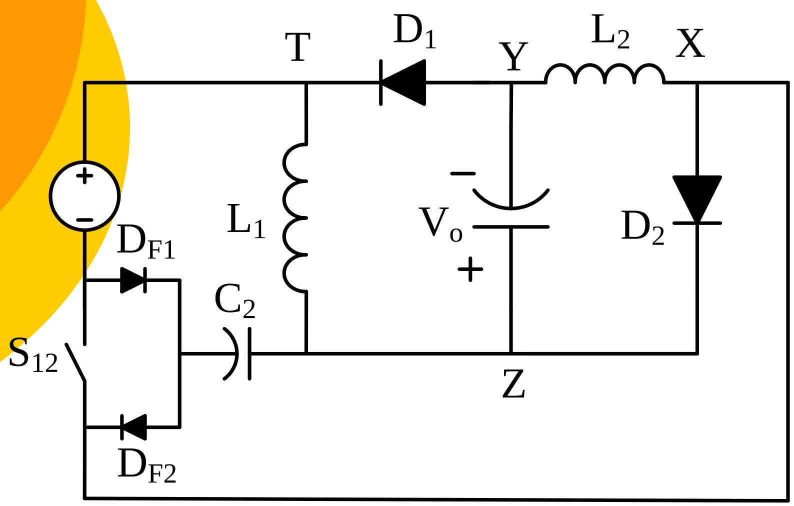
(a)



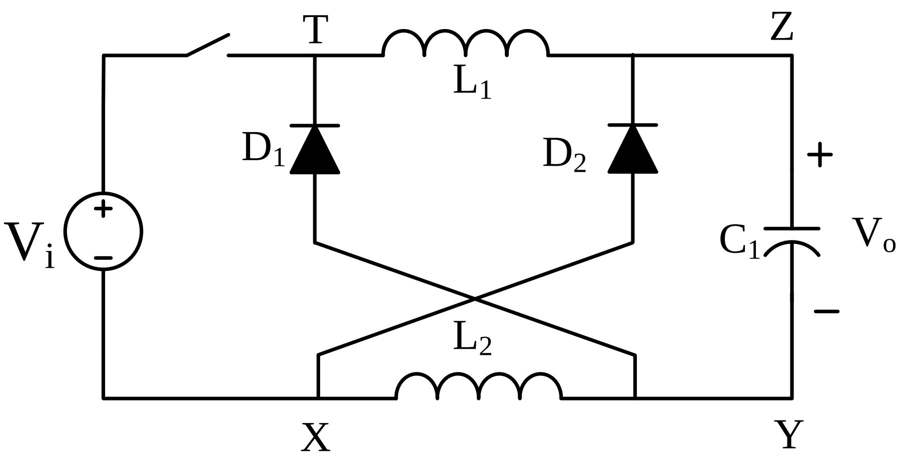
$\Longleftrightarrow$



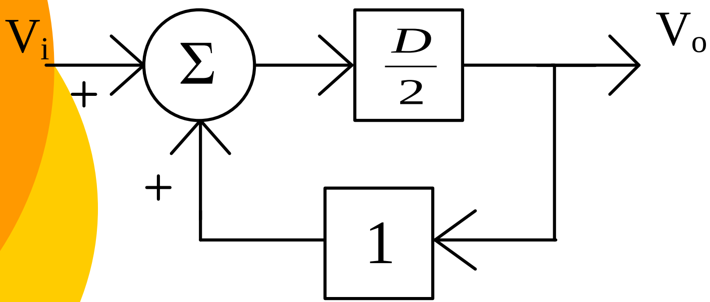
$$\frac{V_o}{V_i} = \frac{D}{2-D}$$



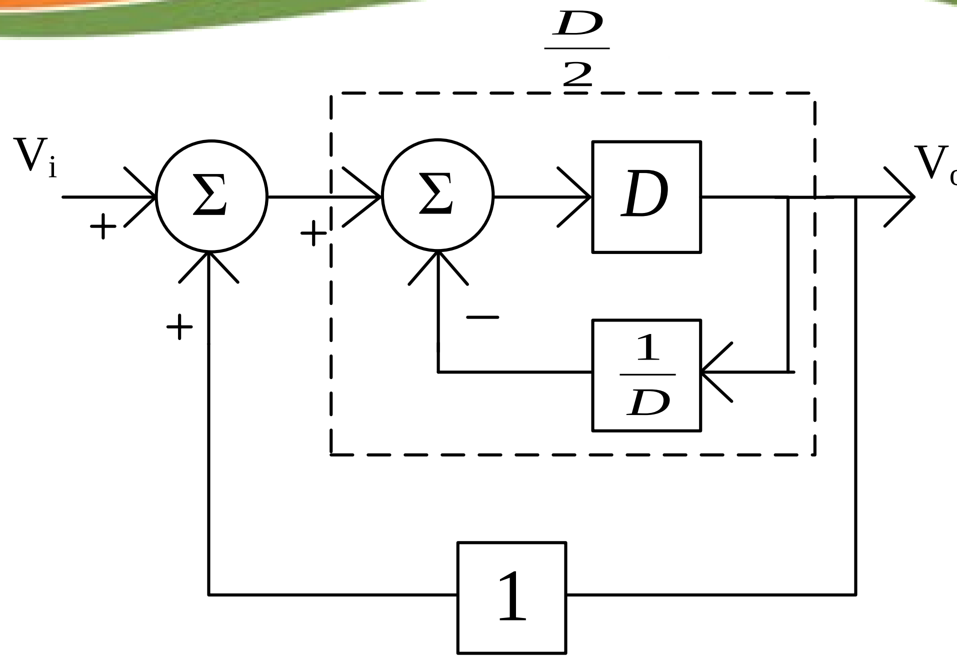
(b)



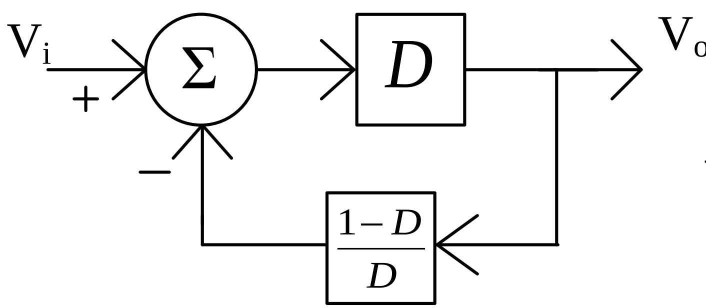
(c) [48]



(a) no converter to realize $\frac{D}{2}$



(b) no converter to realize the negative feedback path of $\frac{1}{D}$



$$\frac{V_o}{V_i} = \frac{D}{2-D}$$

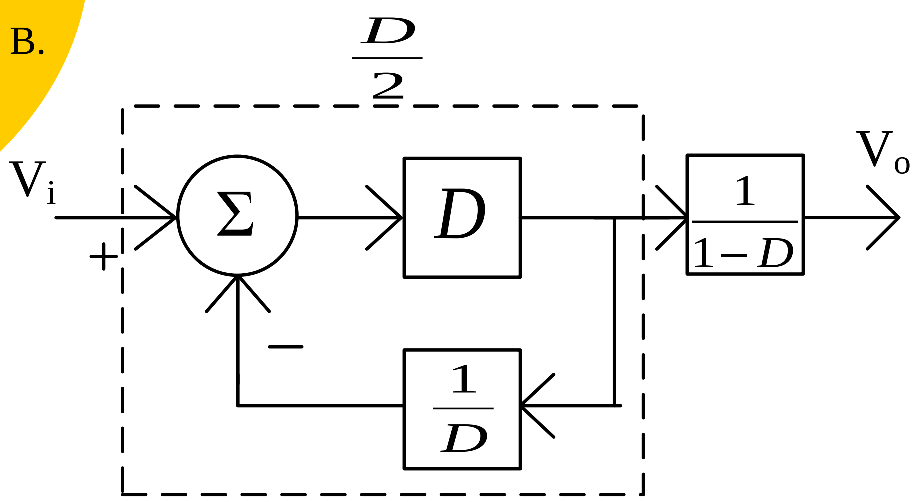
(c) Combine the two feedback paths into a single one.

This block diagram can be synthesized by the converters shown in eg. 1.

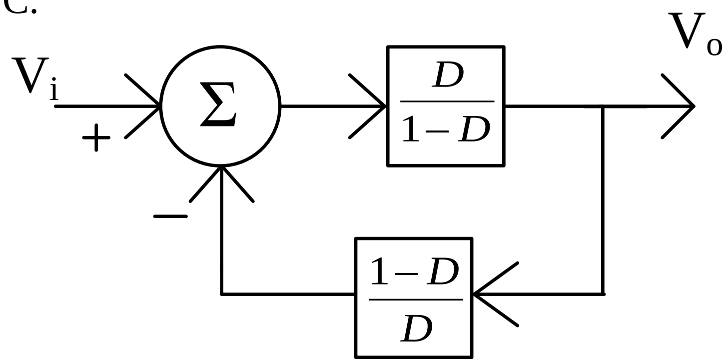
Decoding D/2(1-D)

A. $$\frac{V_o}{V_i} = \frac{D}{2(1-D)} = \frac{D}{2} \times \frac{1}{1-D}$$

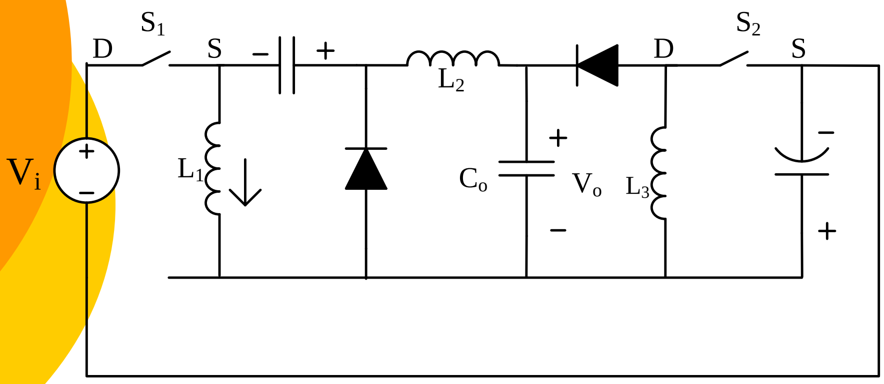
B.



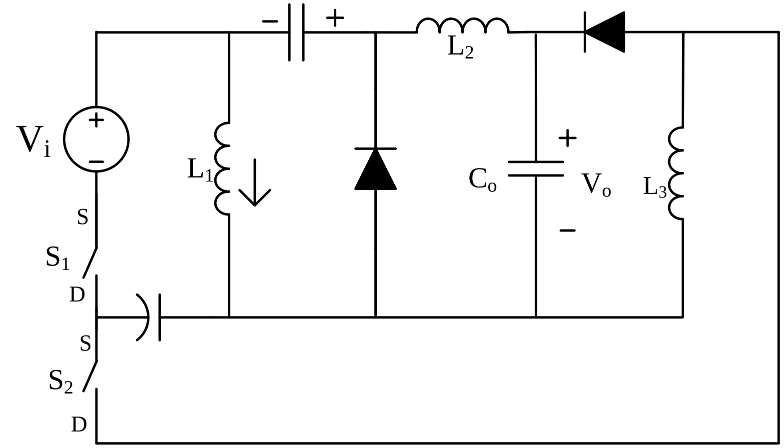
C.



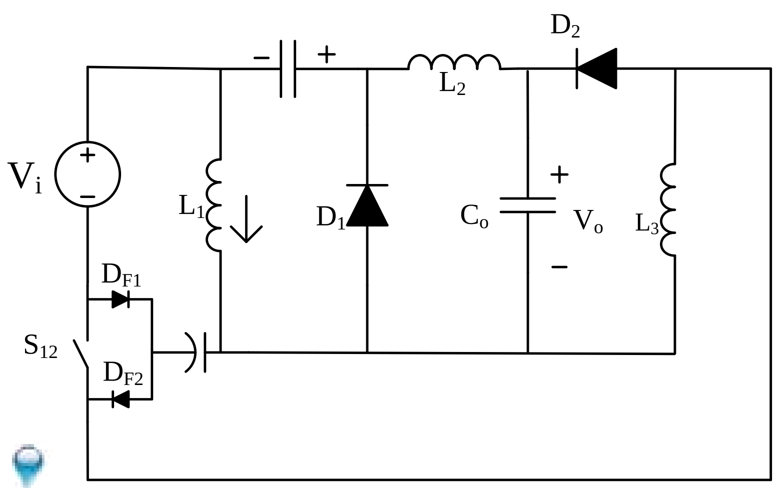
1. Synthesizing with Zeta + I-Buck-Boost



(a)

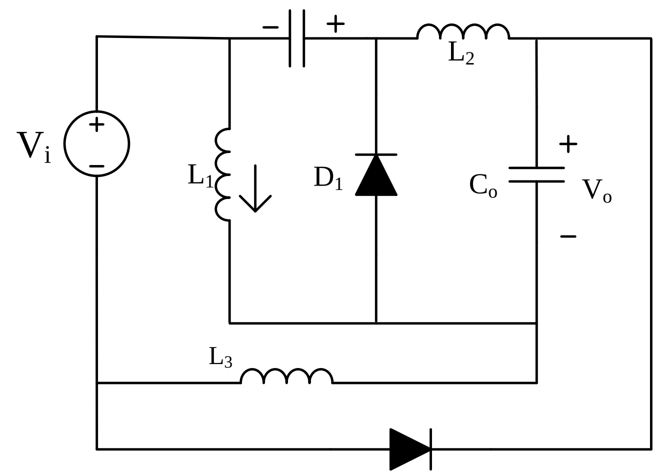


(b)

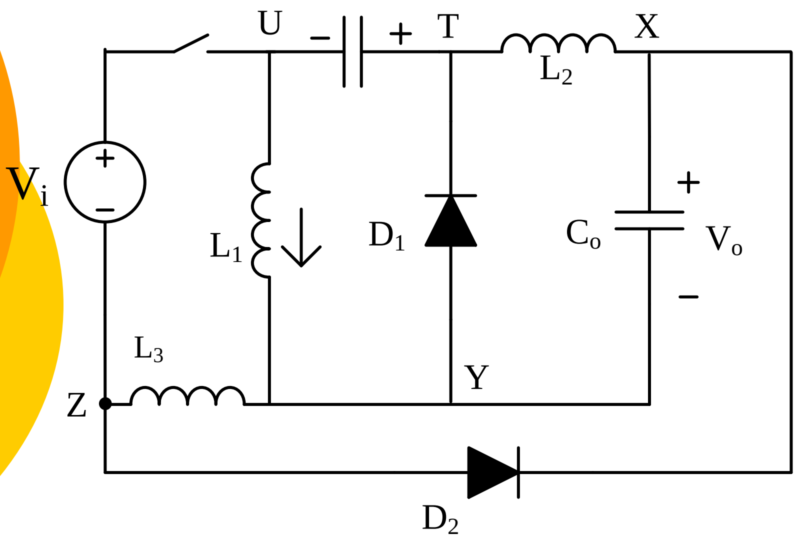


$I_1 = I_2 \rightarrow D_{F1}$ and D_{F2} can be saved

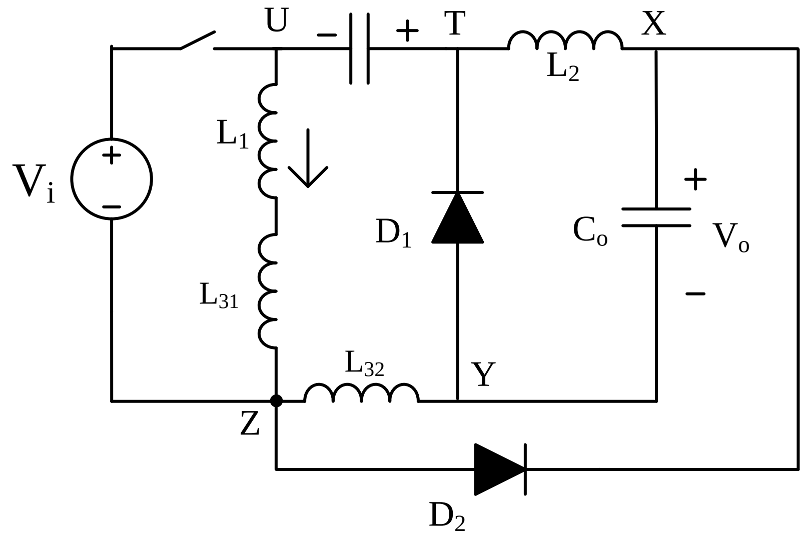
(c)



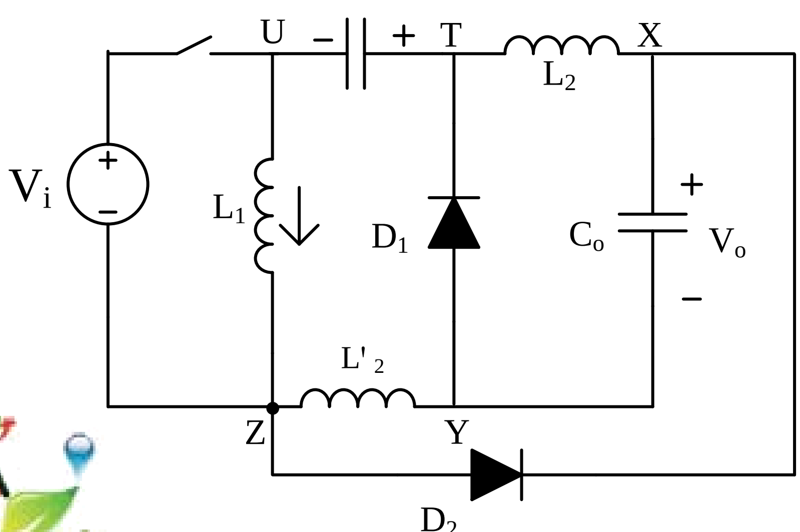
(d)



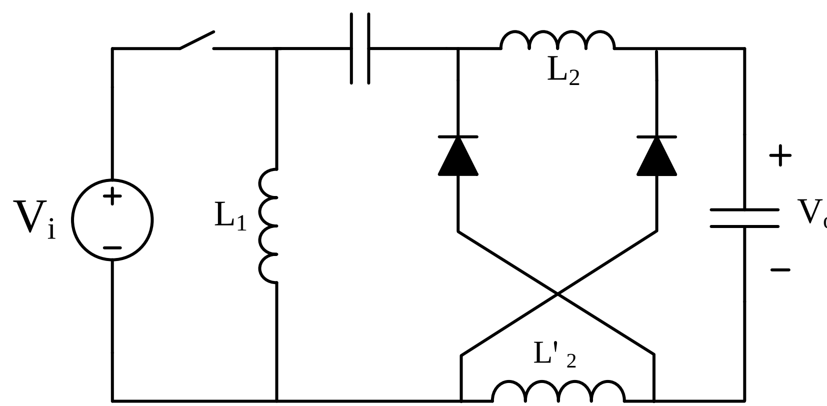
(e)



(f)



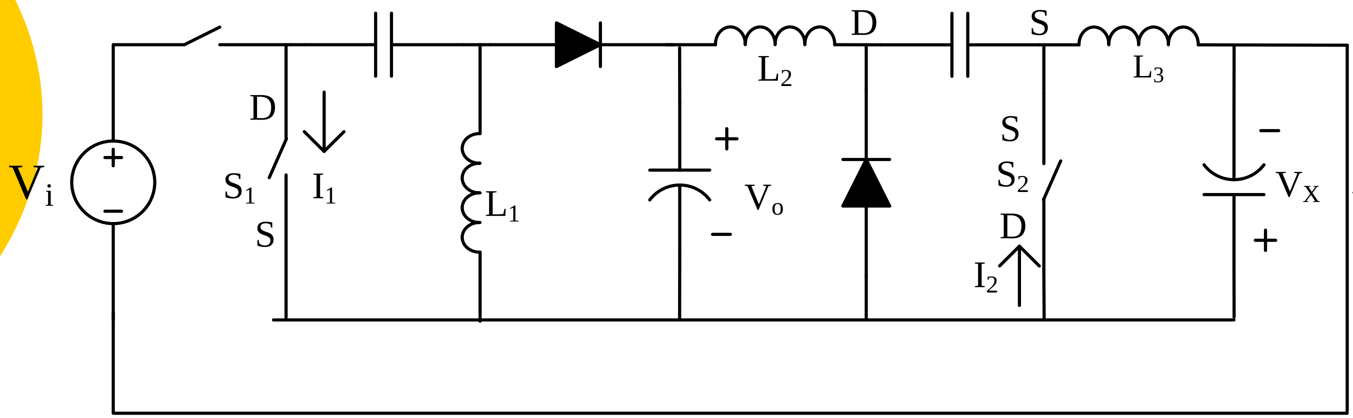
(g)



(h) $$\frac{V_O}{V_i} = \frac{D}{2(1-D)}$$ [48]

2. Synthesizing with SEPIC + I-Ćuk

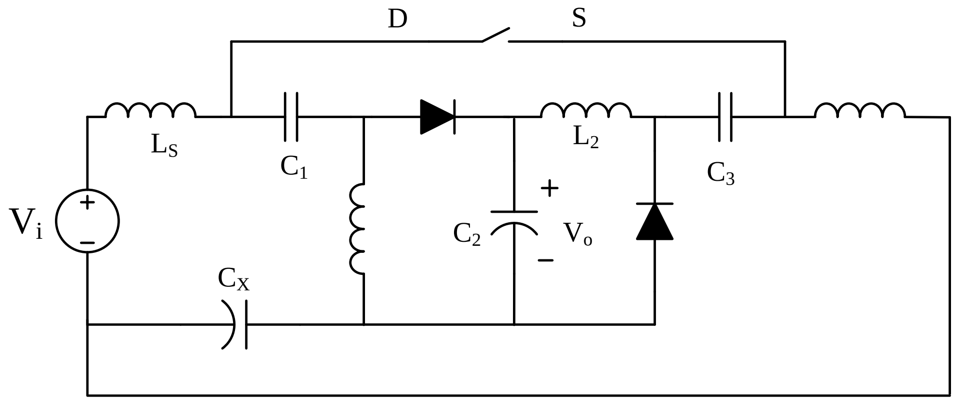
SEPIC+I-Cuk



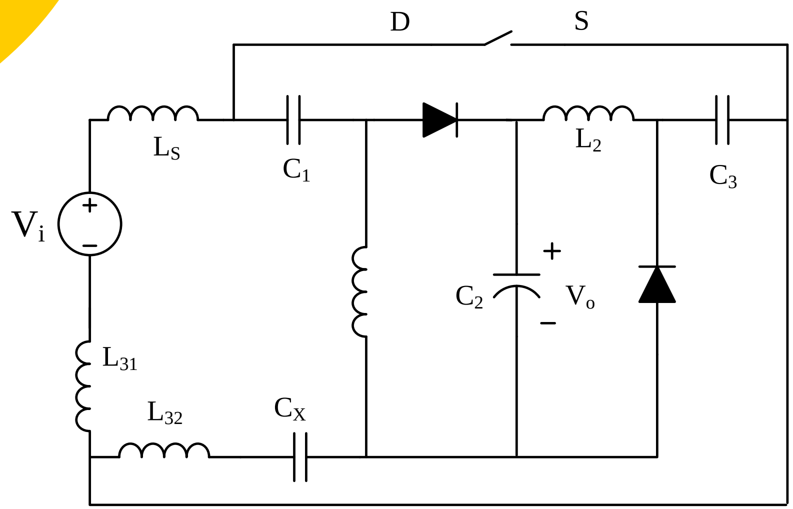
$$V_X = \frac{1}{2}V_i = \frac{1-D}{D}V_O$$

Let $L_S = L_1 = L_2 = L_3$, and we have $I_1 = I_2$

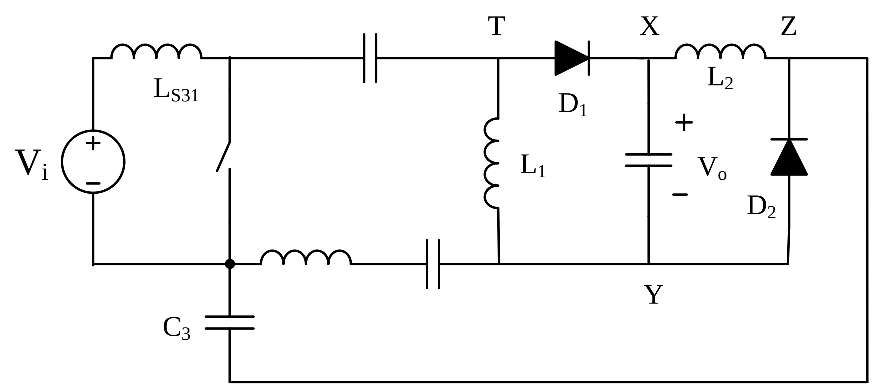
(a)


D
S
L_S
C_1
L_2
C_3
V_i
+
C_2
V_o
−
C_X

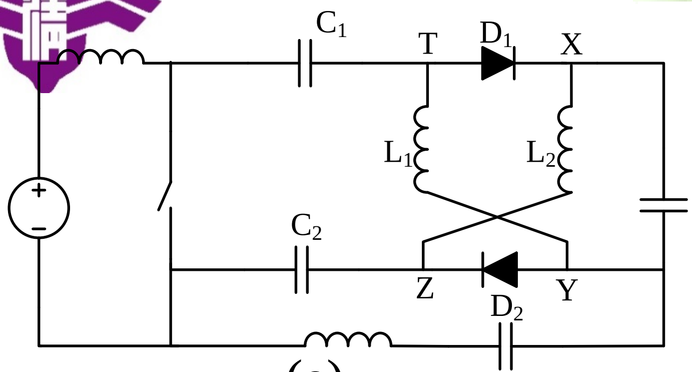
(b)


D
S
L_S
C_1
L_2
C_3
V_i
+
C_2
V_o
−
L_31
L_32
C_X

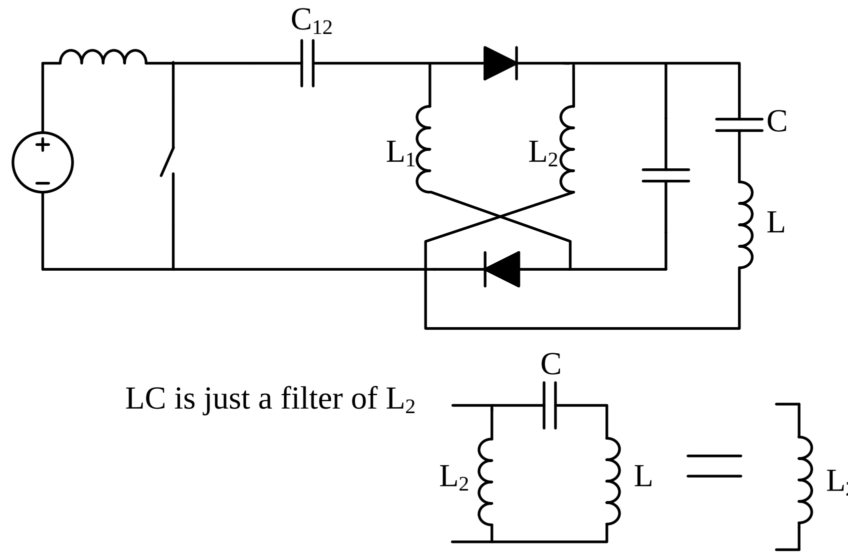
(c)


T
X
Z
L_S31
D_1
L_2
V_i
+
L_1
V_o
−
D_2
Y
C_3

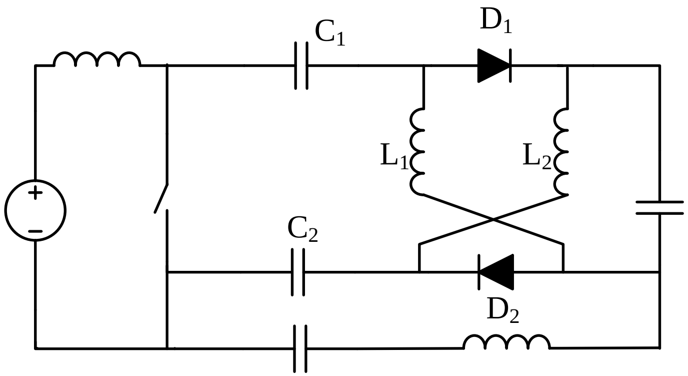
(d)



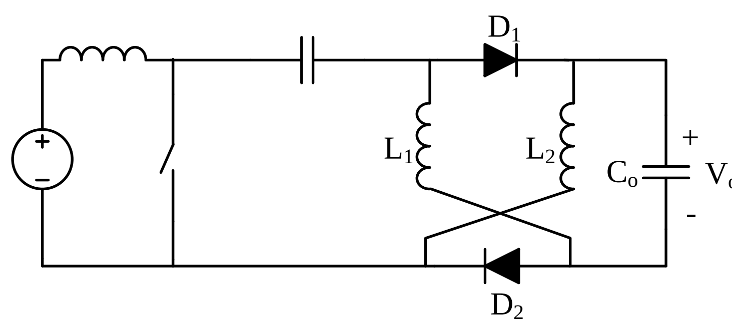
(e)



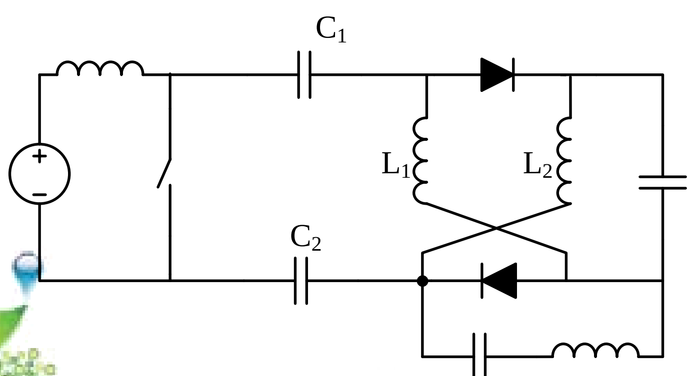
(h)



(f)

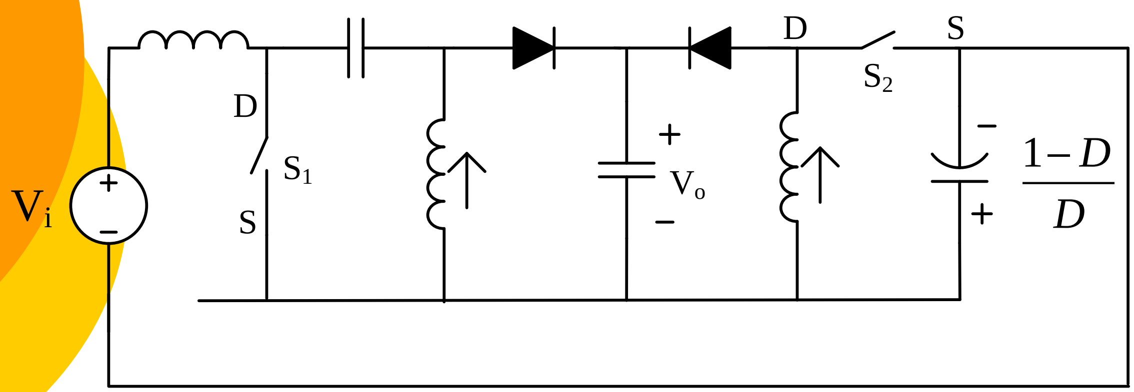


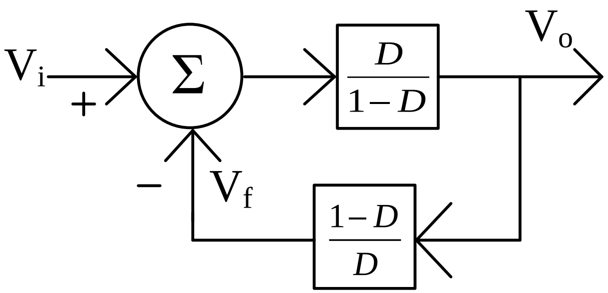
(i) $$\frac{V_O}{V_i} = \frac{D}{2(1-D)}$$ [48]



(g)

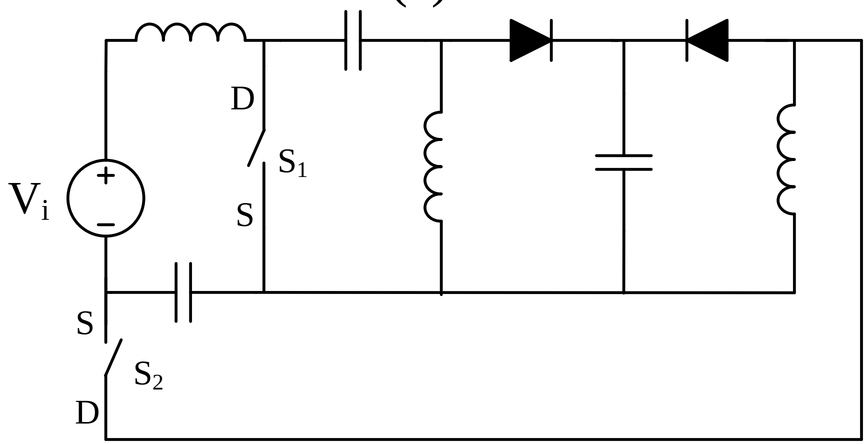
3. Synthesizing with SEPIC + I-Buck-Boost





$$\frac{V_O}{V_i} = \frac{D}{2(1-D)}$$

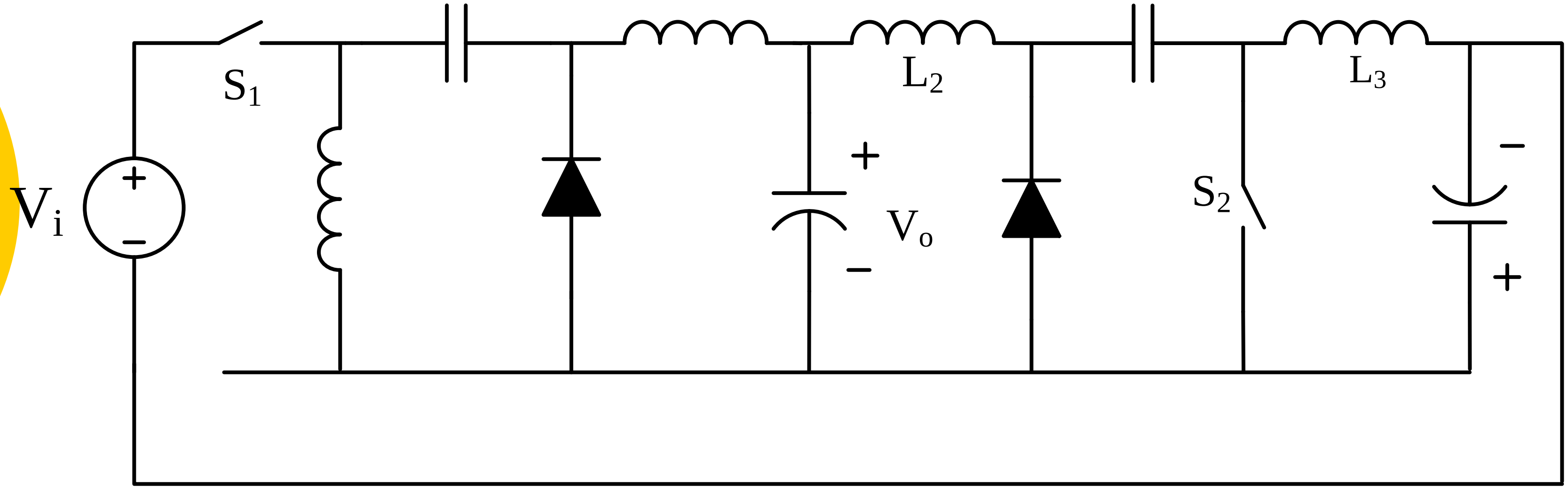
(a)



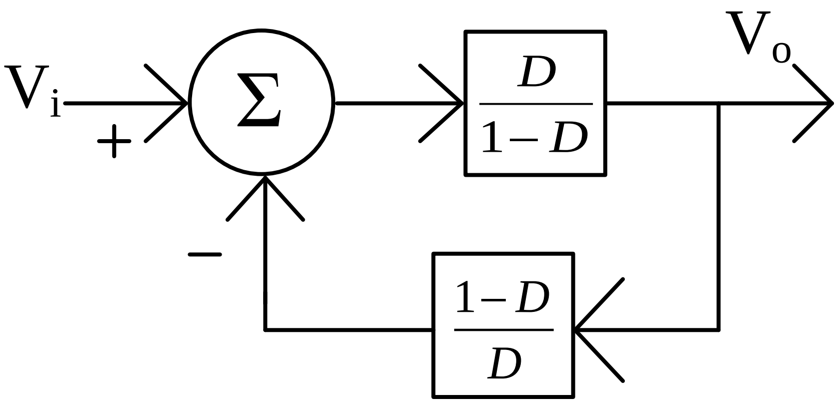
No common node between S_1 and S_2

(b)

4. Synthesizing with Zeta + I-Ćuk

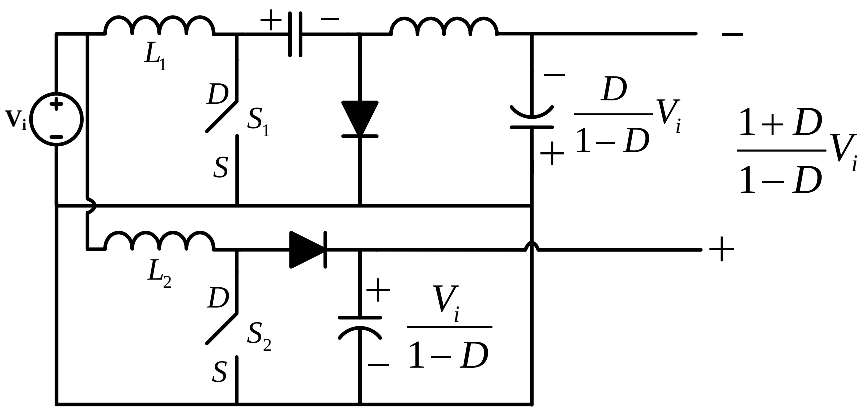


No common node between S_1 and S_2



Decoding (1+D)/(1-D)

Synthesizing with Ćuk + Boost

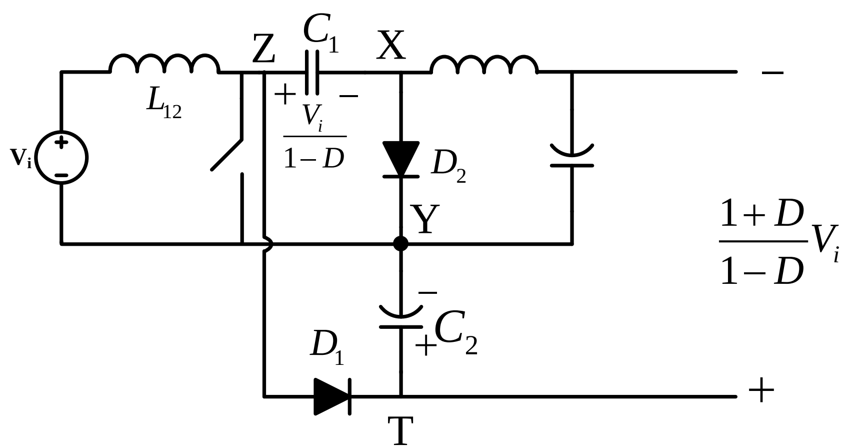


$$\frac{V_O}{V_i} = \frac{1+D}{1-D}$$

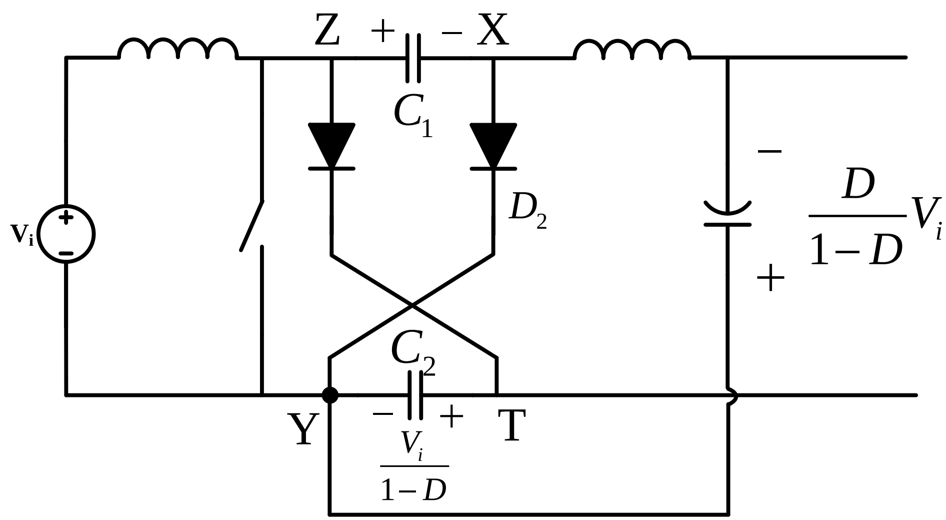
$$\Longrightarrow V_O = \frac{1}{1-D}V_i + \frac{D}{1-D}V_i$$

=Boost+Cuk

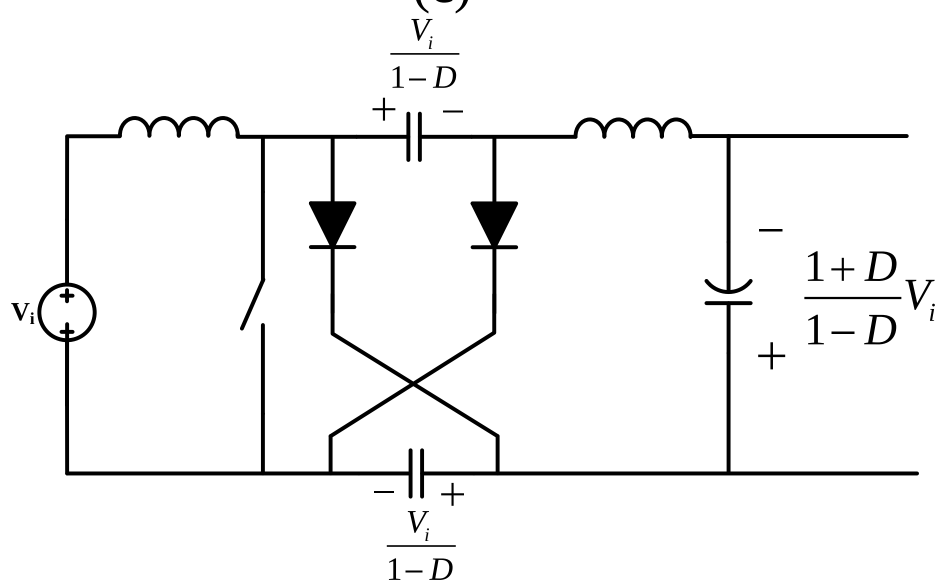
(a)



(b)

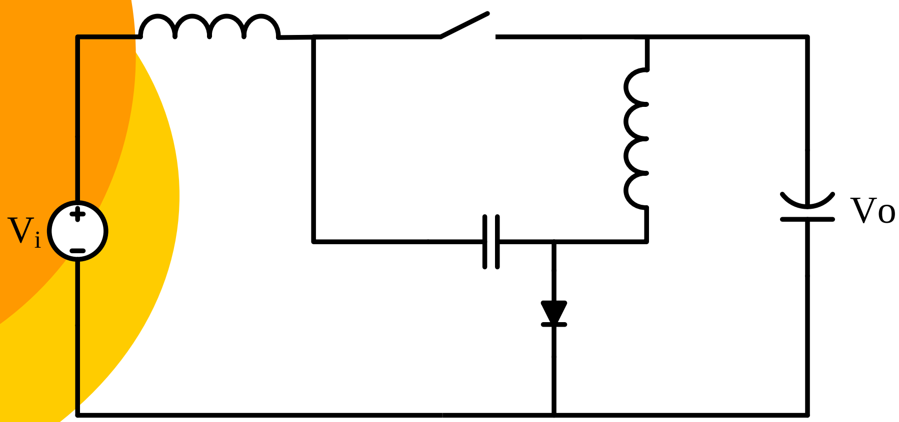

Z
X
C_1
D_2
v_i
$\frac{D}{1-D}V_i$
C_2
Y
T
$\frac{V_i}{1-D}$

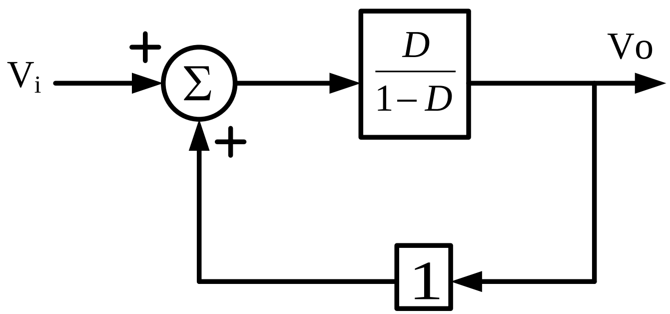
(c)


$\frac{V_i}{1-D}$
v_i
$\frac{1+D}{1-D}V_i$
$\frac{V_i}{1-D}$

(d) [48]

Decoding D/(1-2D)





$$\frac{V_o}{V_i}=\frac{D}{1-2D}\Rightarrow(1-2D)V_o=DV$$

$$\Rightarrow V_o(1-D)=(V_i+V_o)D$$

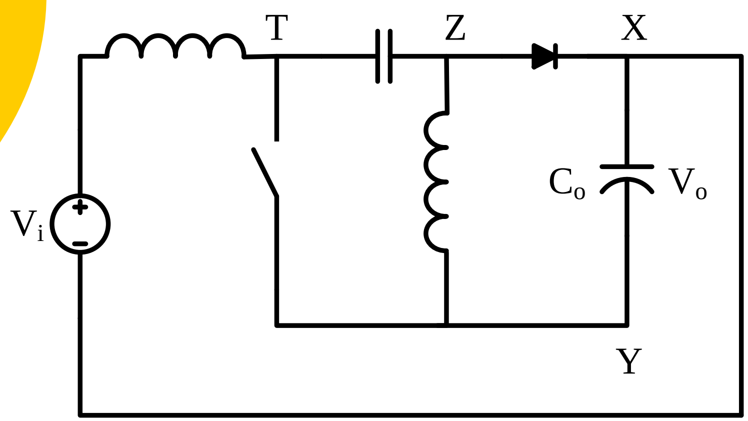
$$\Rightarrow V_o=\frac{(V_i+V_o)D}{1-D}$$

$$=\frac{V_iD}{1-D}+\frac{V_oD}{1-D}$$

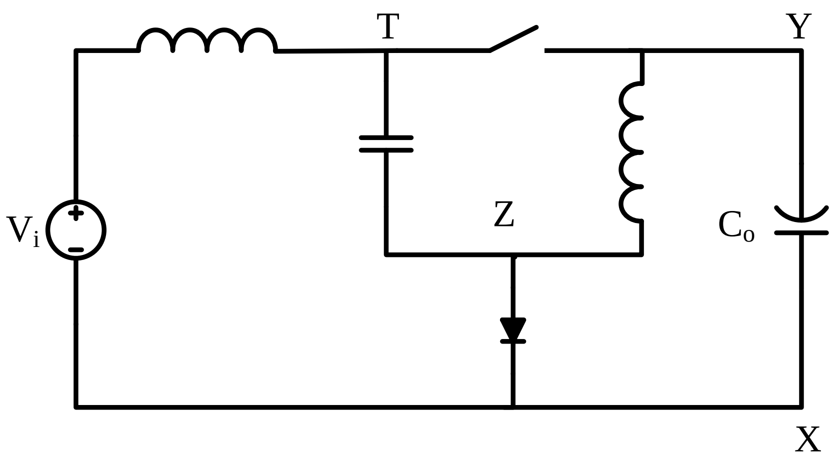
$$\Rightarrow V_o\left(1-\frac{D}{1-D}\right)=V_i\left(\frac{D}{1-D}\right)$$

$$\Rightarrow\frac{V_o}{V_i}=\frac{\dfrac{D}{1-D}}{1-\dfrac{D}{1-D}}$$

Synthesizing with SEPIC + positive feedback



(a)



(b) [29]

Synthesizing PWM Converters

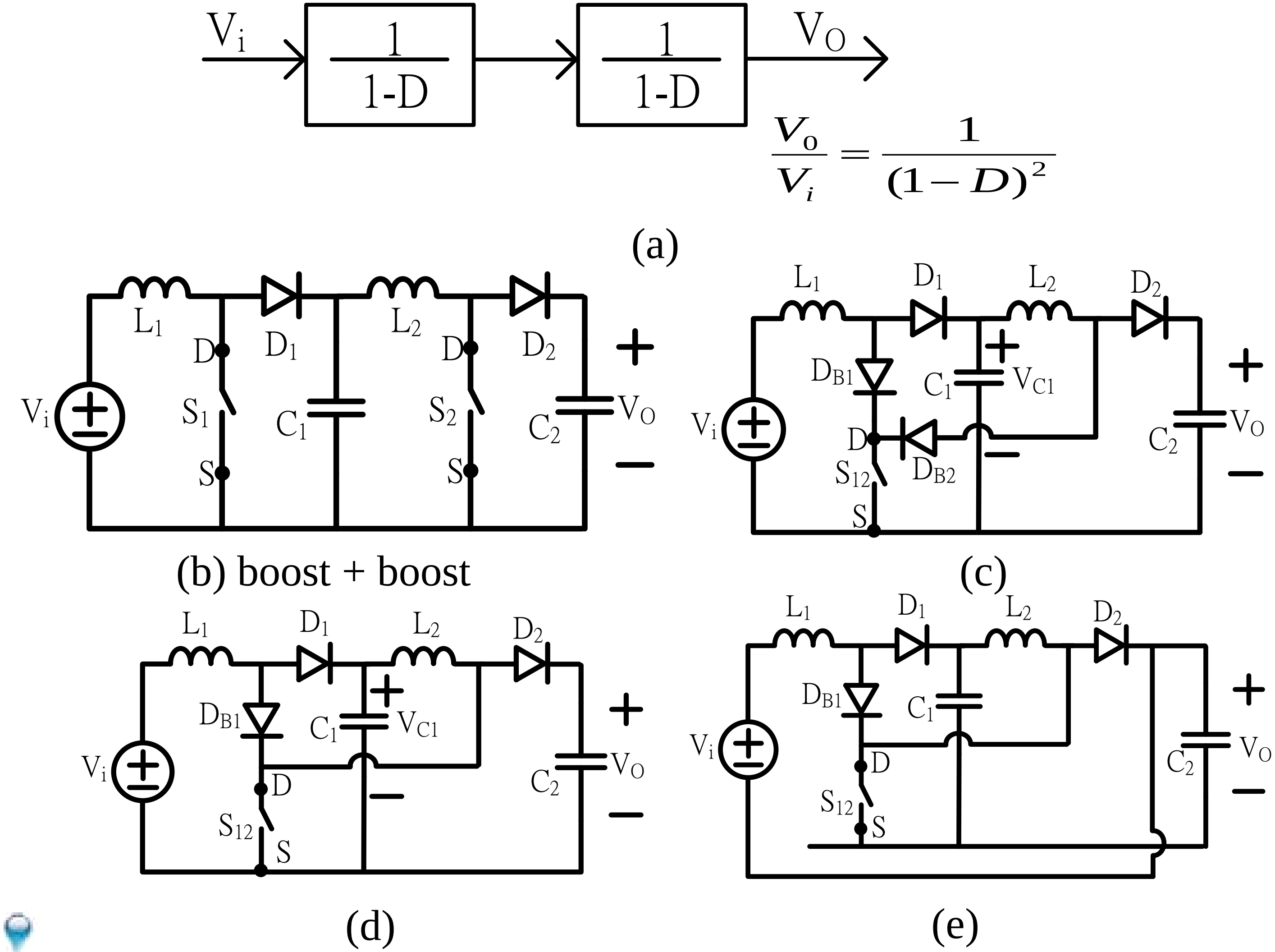
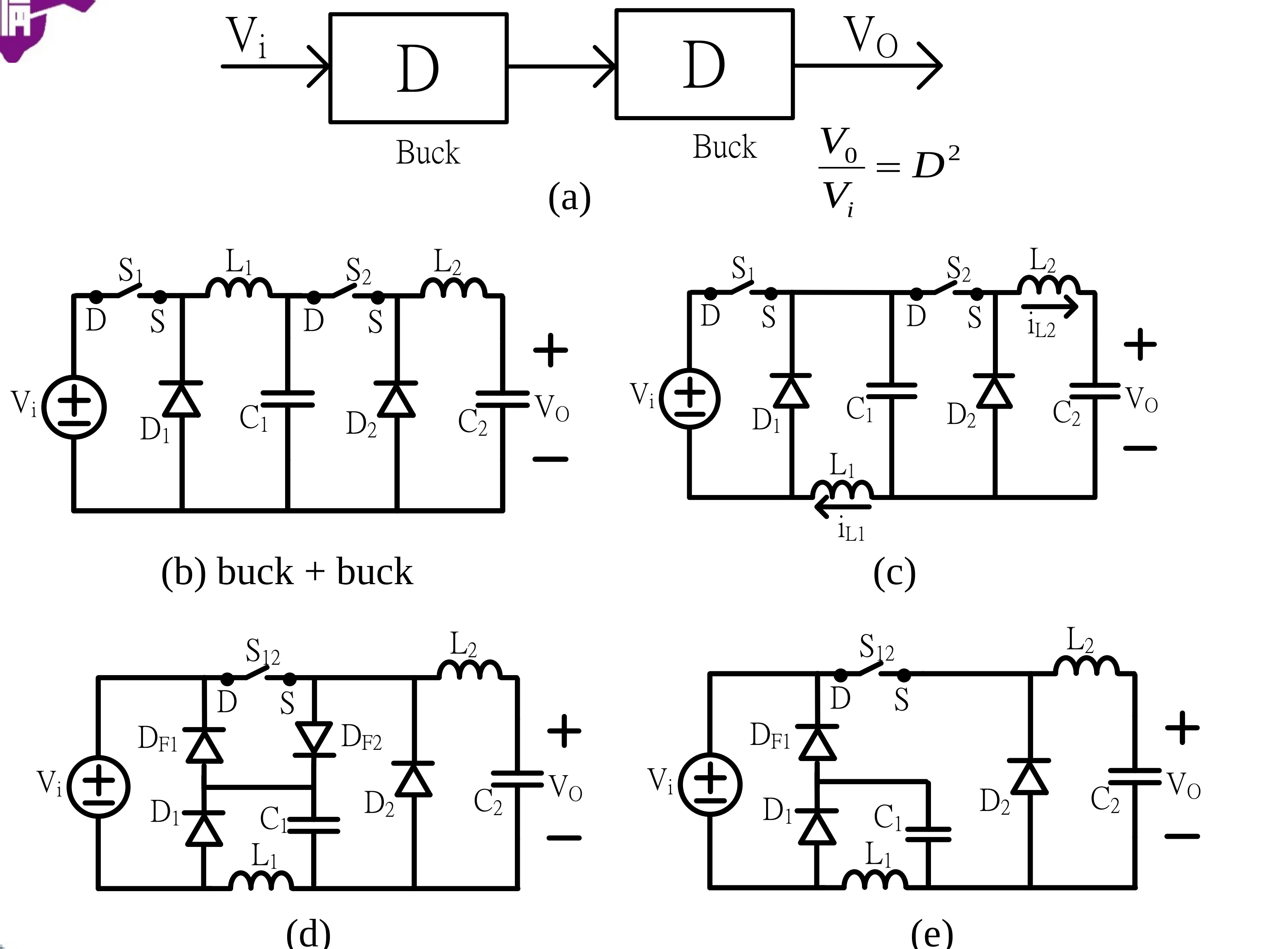


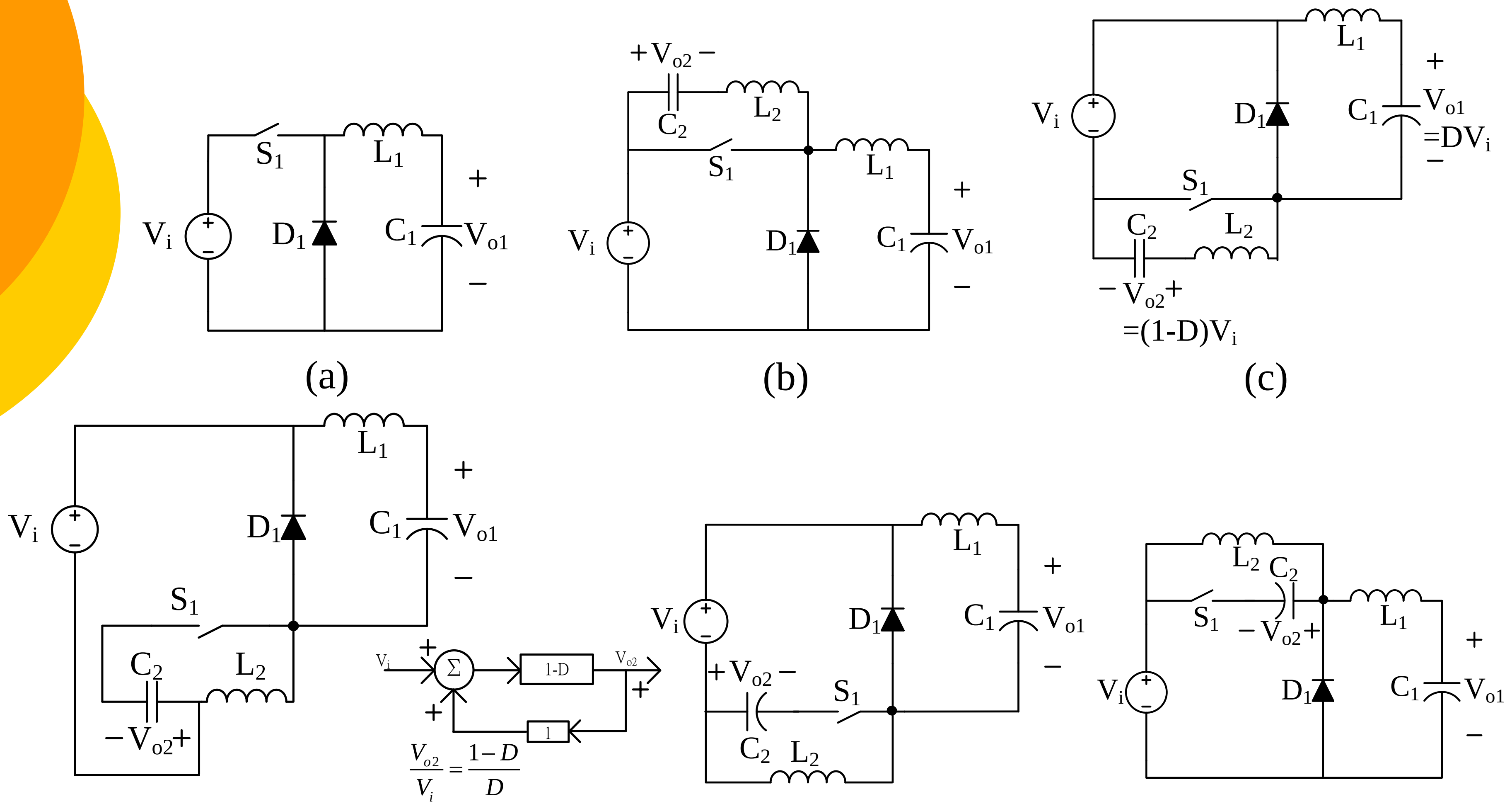
Fig. 27. Decoding and evolution of the boost-boost grafted PWM converter from two boost converters in cascade.



$$\frac{V_o}{V_i} = D^2$$

Fig. 28. Decoding and evolution of the buck-buck grafted PWM converter from two buck converters in cascade.

➢ Buck Converter with a Second Output V_{o2}

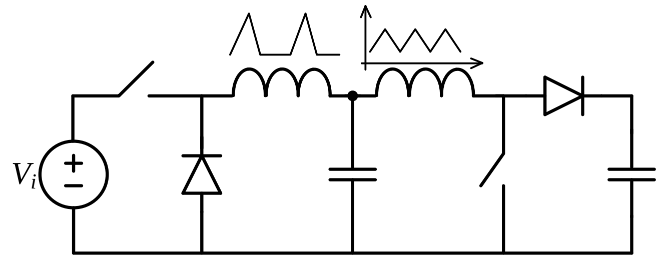


(a) (b) (c)

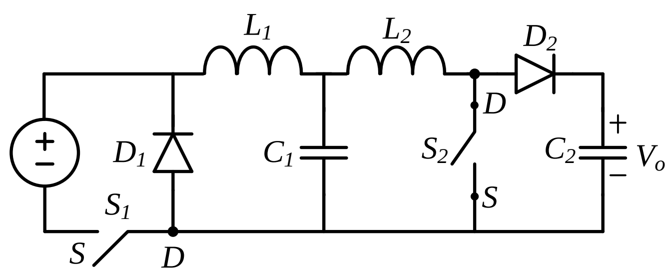
(d) (e) $V_{o2}/V_i=(1-D)/D$ (f) $V_{o2}/V_i=(1-D)/D$

A. Buck (DCM) + Boost (CCM)

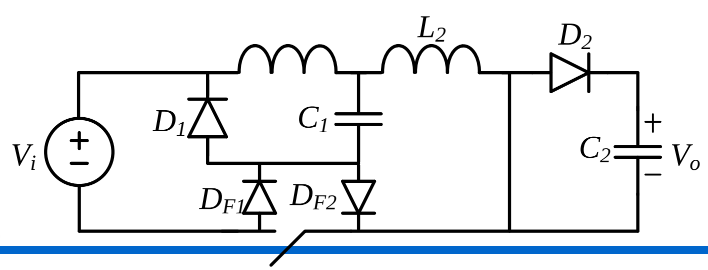
$$\frac{d_1}{(d_1+d_2)} \times \frac{1}{(1-d_2)} = \frac{d_1}{(d_1+d_2)(1-d_2)}$$



(a)



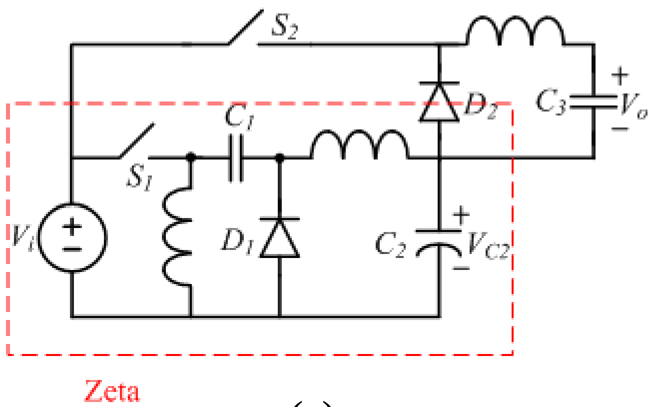
(b)



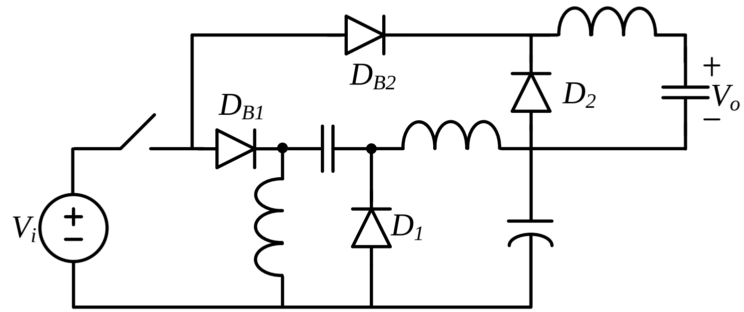
(c)

B. Zeta cascoded with Buck

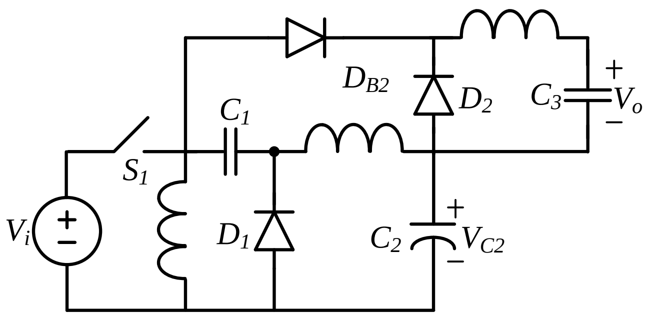
$$\frac{V_o}{V_i} = \left(1 - \frac{D}{1-D}\right) \times D = \left(\frac{1-2D}{1-D}\right) \times D$$



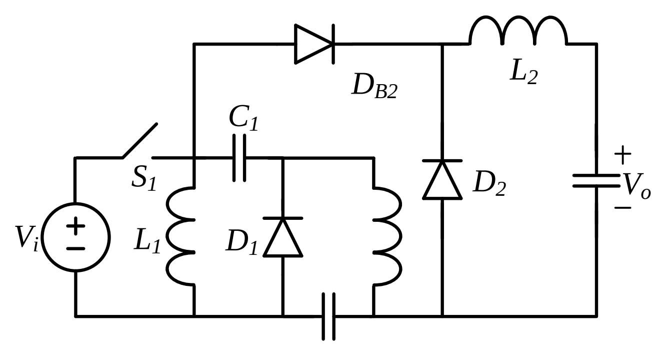
(a)



(b)



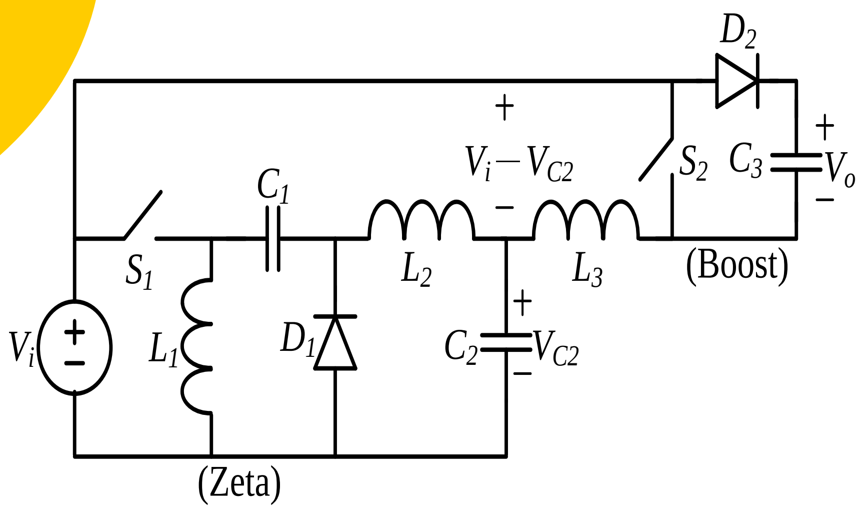
(c)



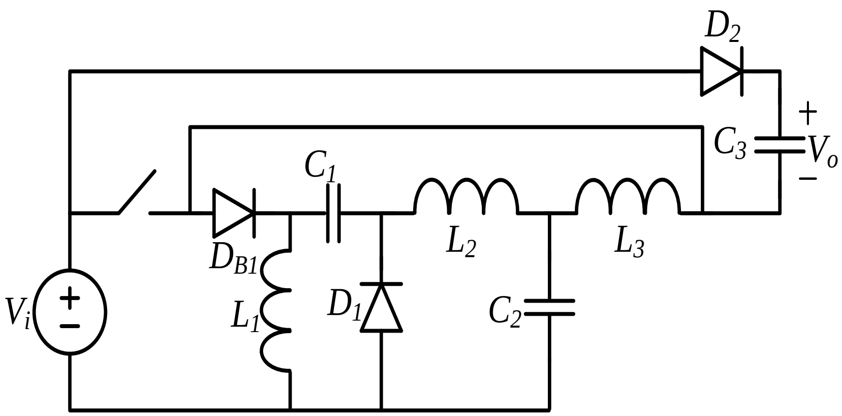
(d)

C. Zeta cascoded with Boost

$$\frac{V_o}{V_i} = \left(1 - \frac{D}{1-D}\right) \times \frac{1}{(1-D)} = \frac{1-2D}{(1-D)^2}$$



(a)



(b)

VII. Other PWM Converters

➢ PWM Converters with DC-transformer

A. Buck-Derived Circuits [3]

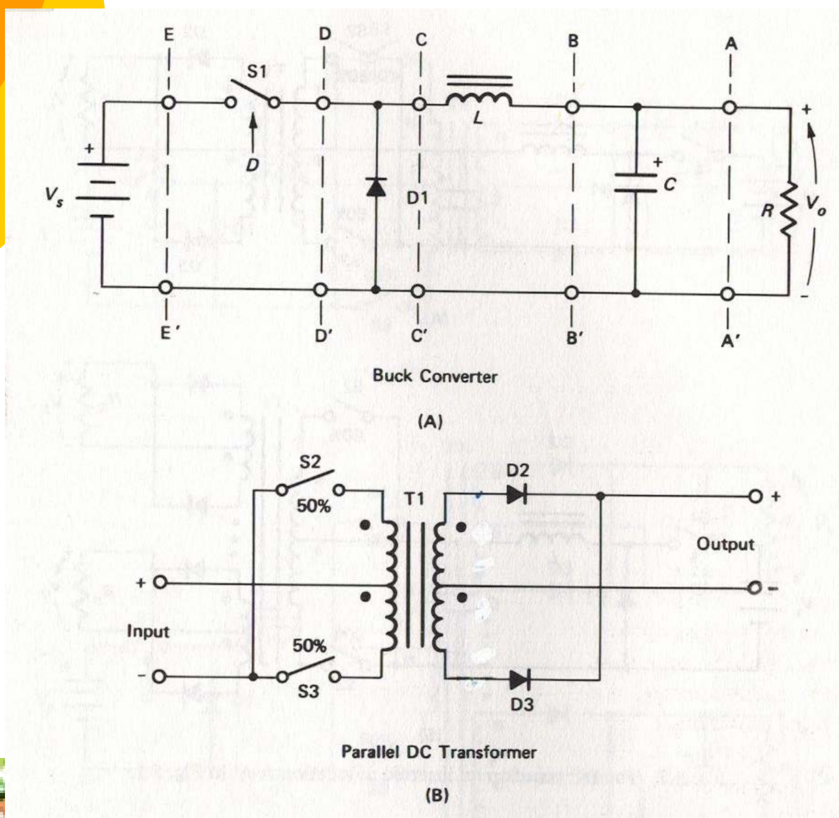


Fig. 5.1. The basic constituents of buck-derived converter circuits.

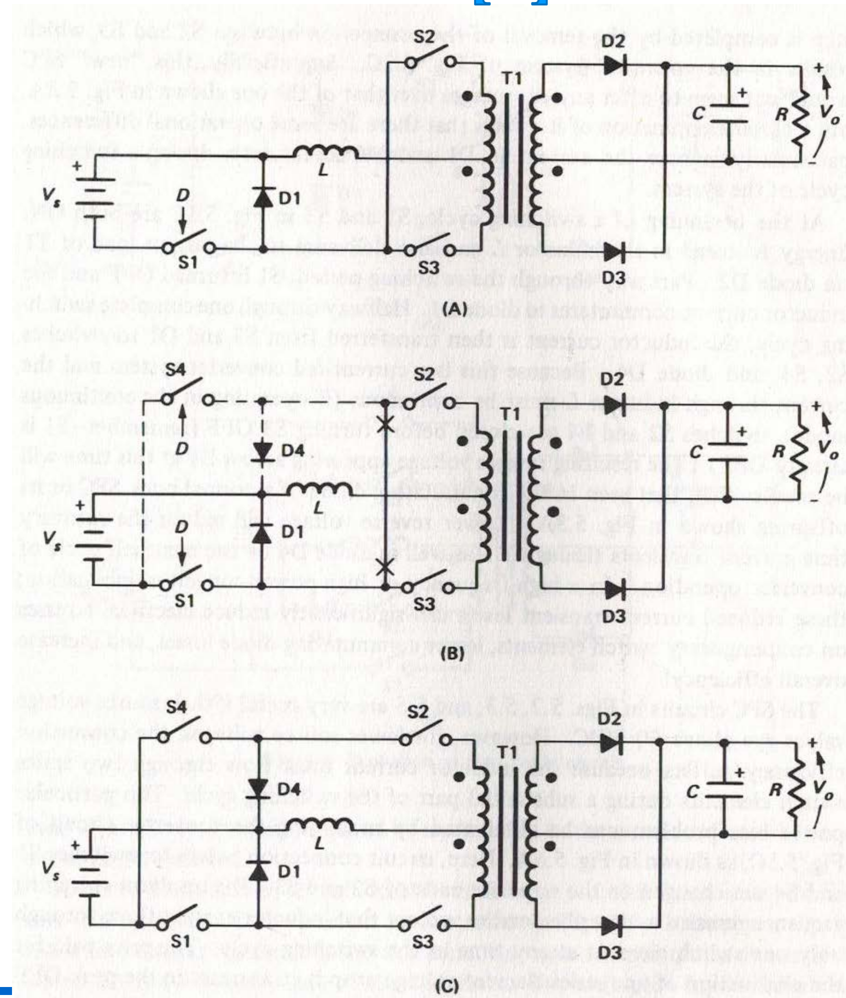
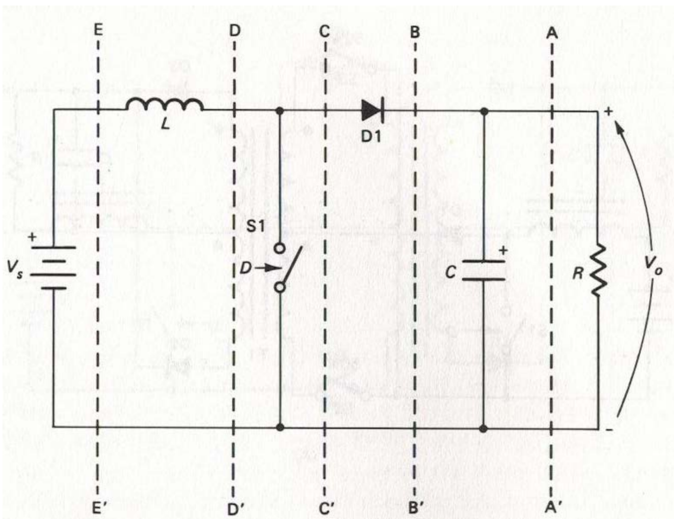


Fig. 5.5. Evolution of the IBM circuit.

B. Boost-Derived Circuits [3]



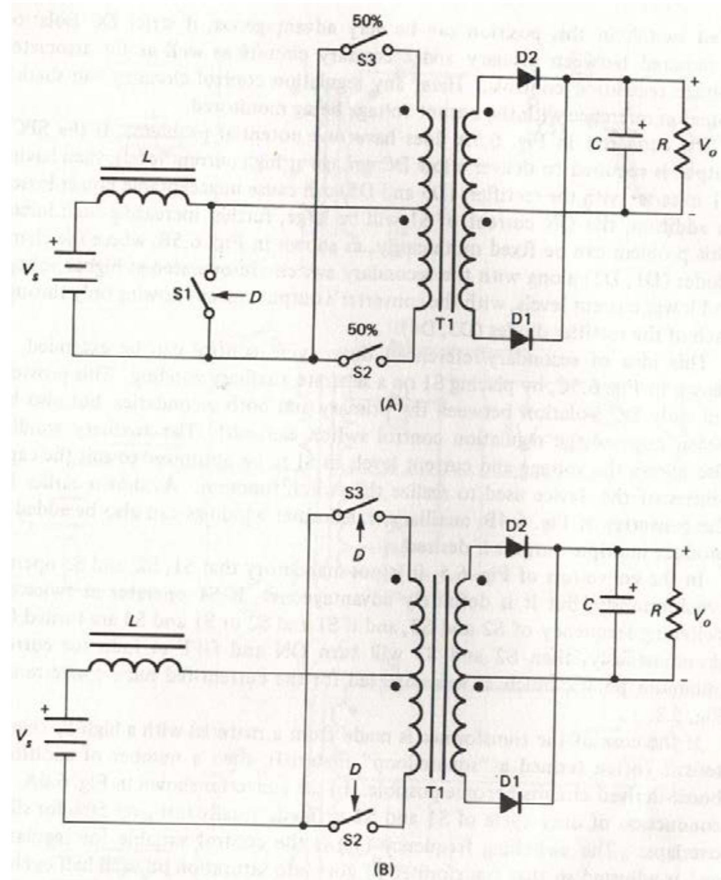
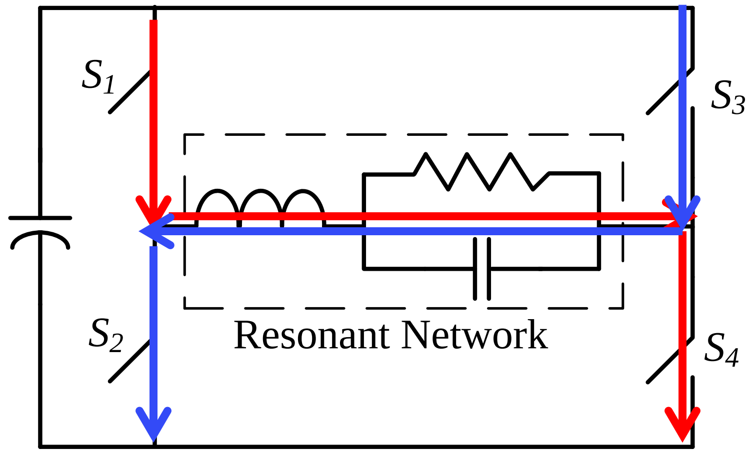
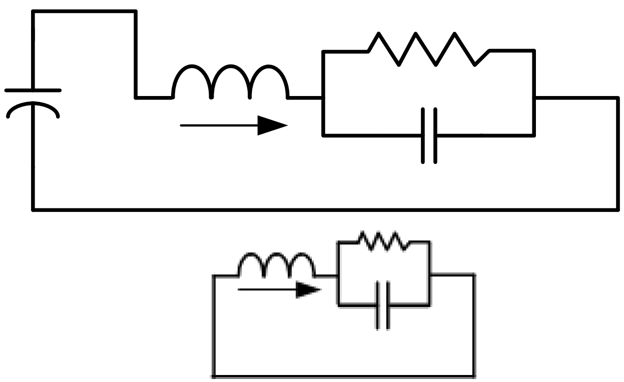


Fig. 6.4. The Clarke circuit.

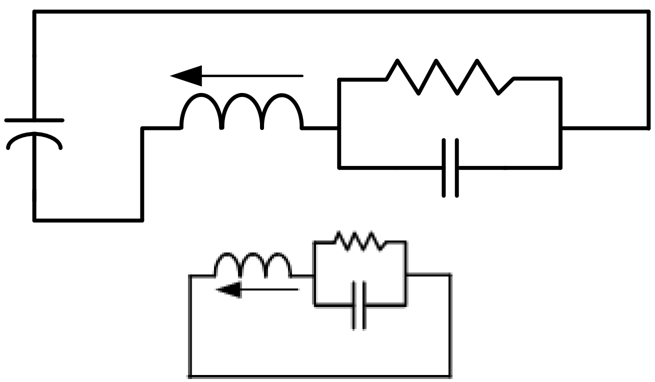
Resonant Converters



(a) Two buck converters in DCM operation

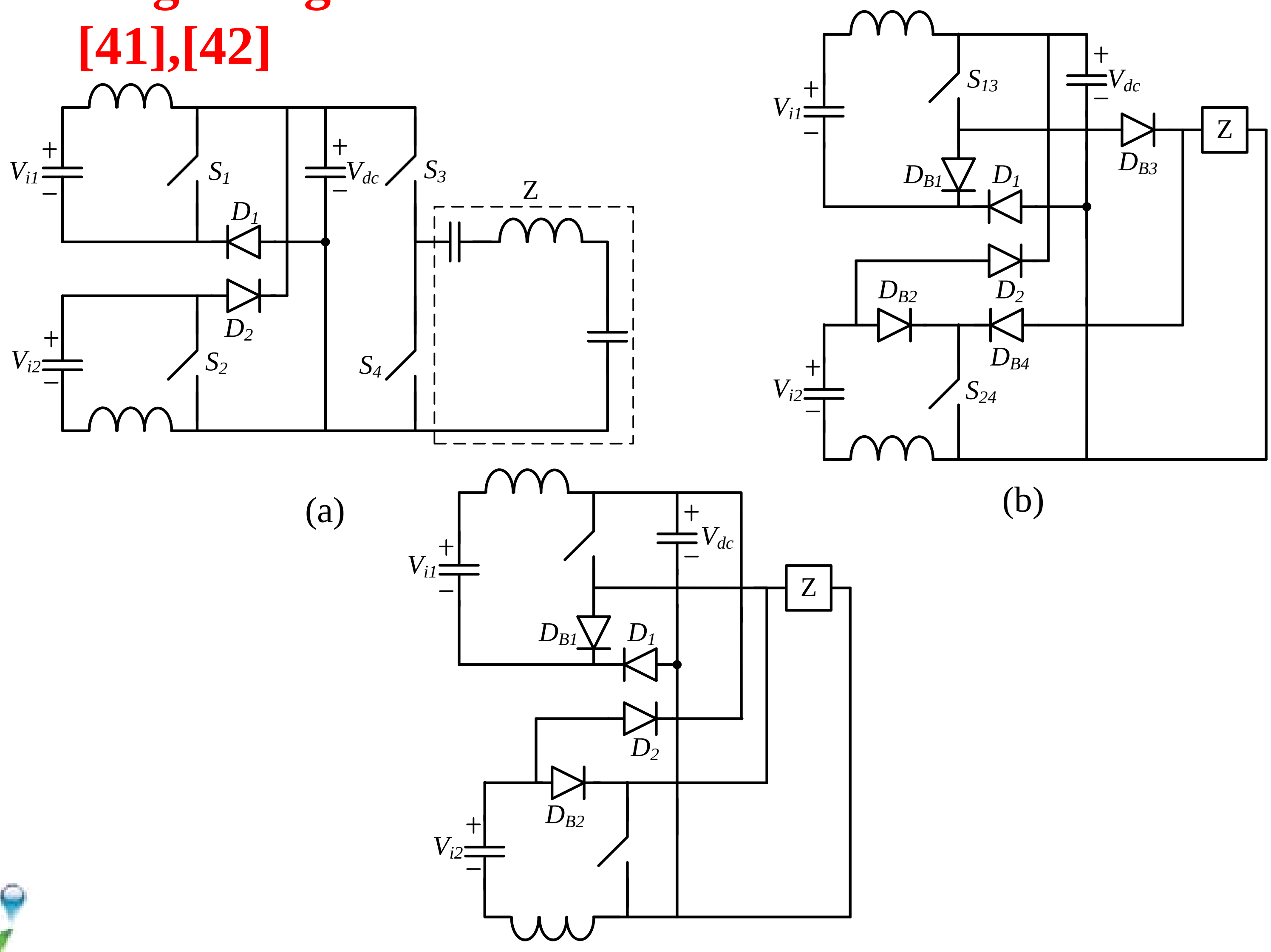


(b) Positive half cycle

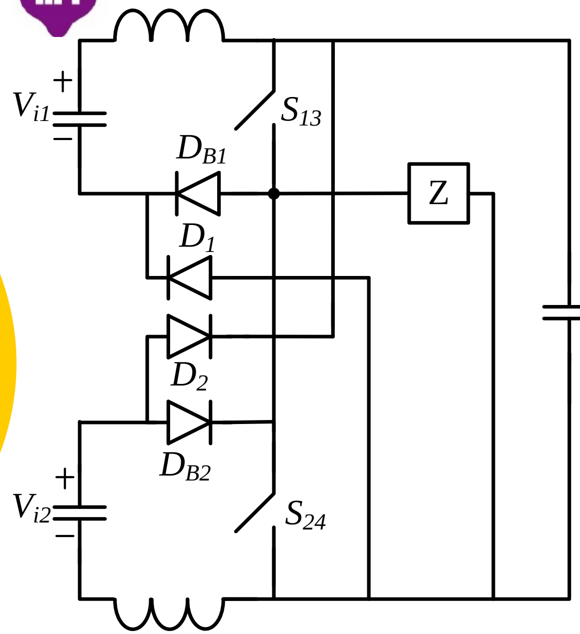


(c) Negative half cycle

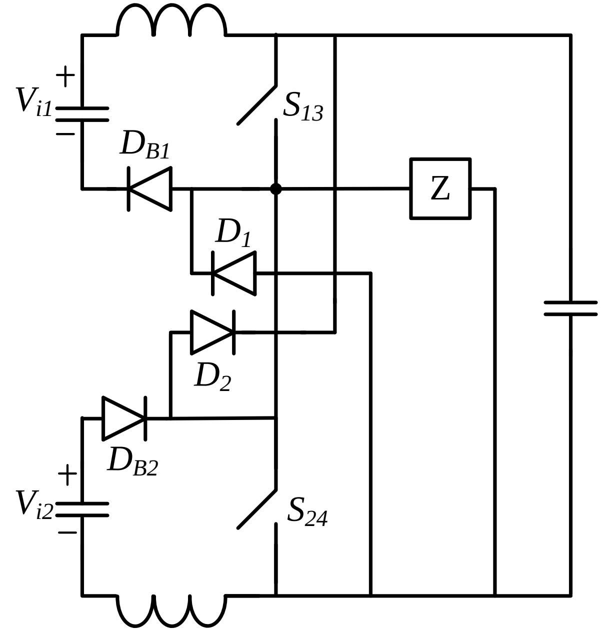
➢ Single-stage Interleaved with Grafted Switch and Diode [41],[42]



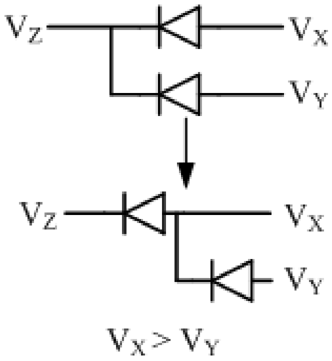
(c). Boost in DCM, and $V_{dc} > V_{i1}$ or $V_{dc} > V_{i2}$

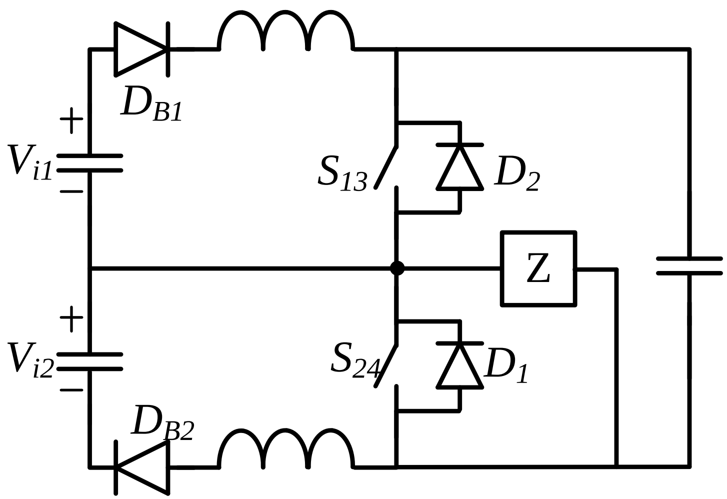


(d)



(e)





(f) D_1 and D_2 are the body diodes of switches S_{24} and S_{13}, respectively.

Interleaved Single-Stage High PFC [43] – Buck + Zeta (with isolation)

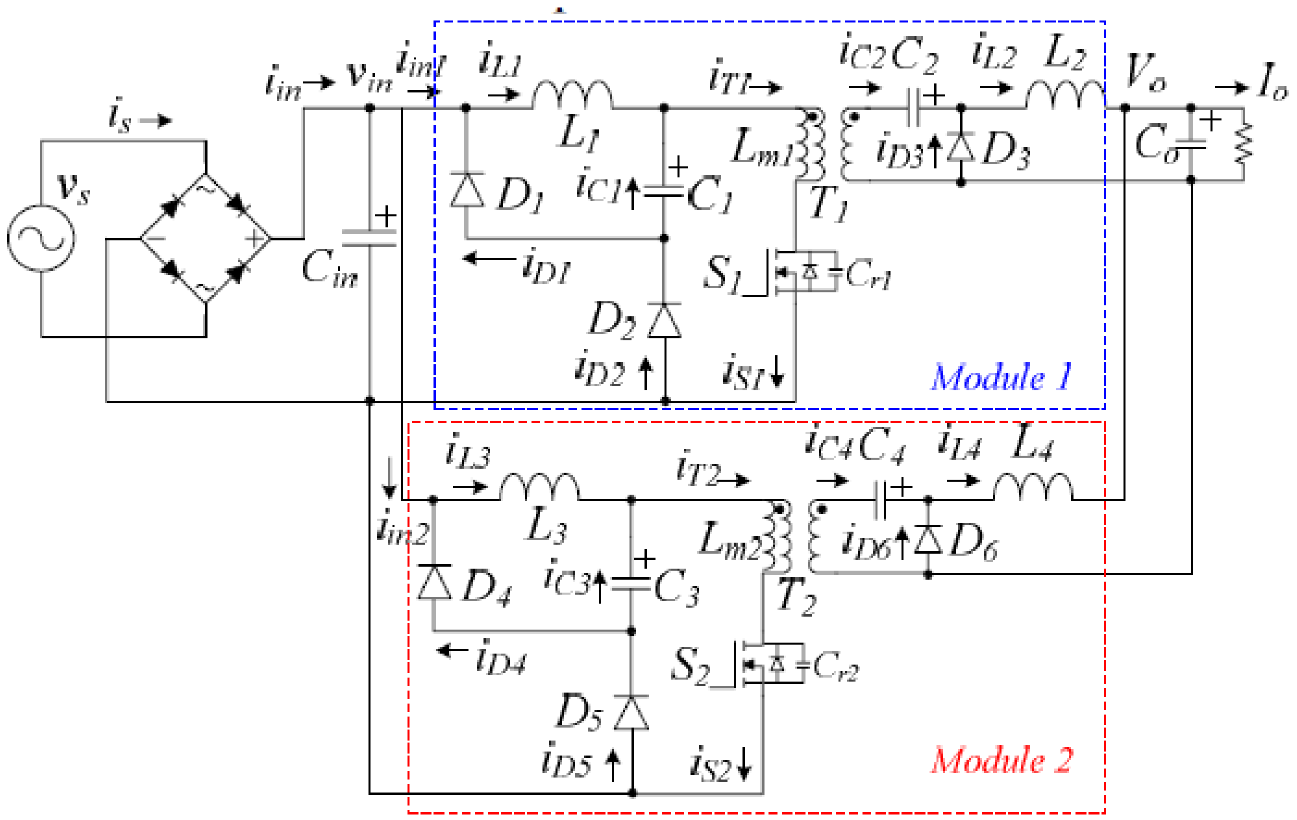


Fig. 1 Circuit configuration of the proposed converter.

Interleaved Single-Stage Full-Bridge Converter [44] – Boost+ Full-Bridge

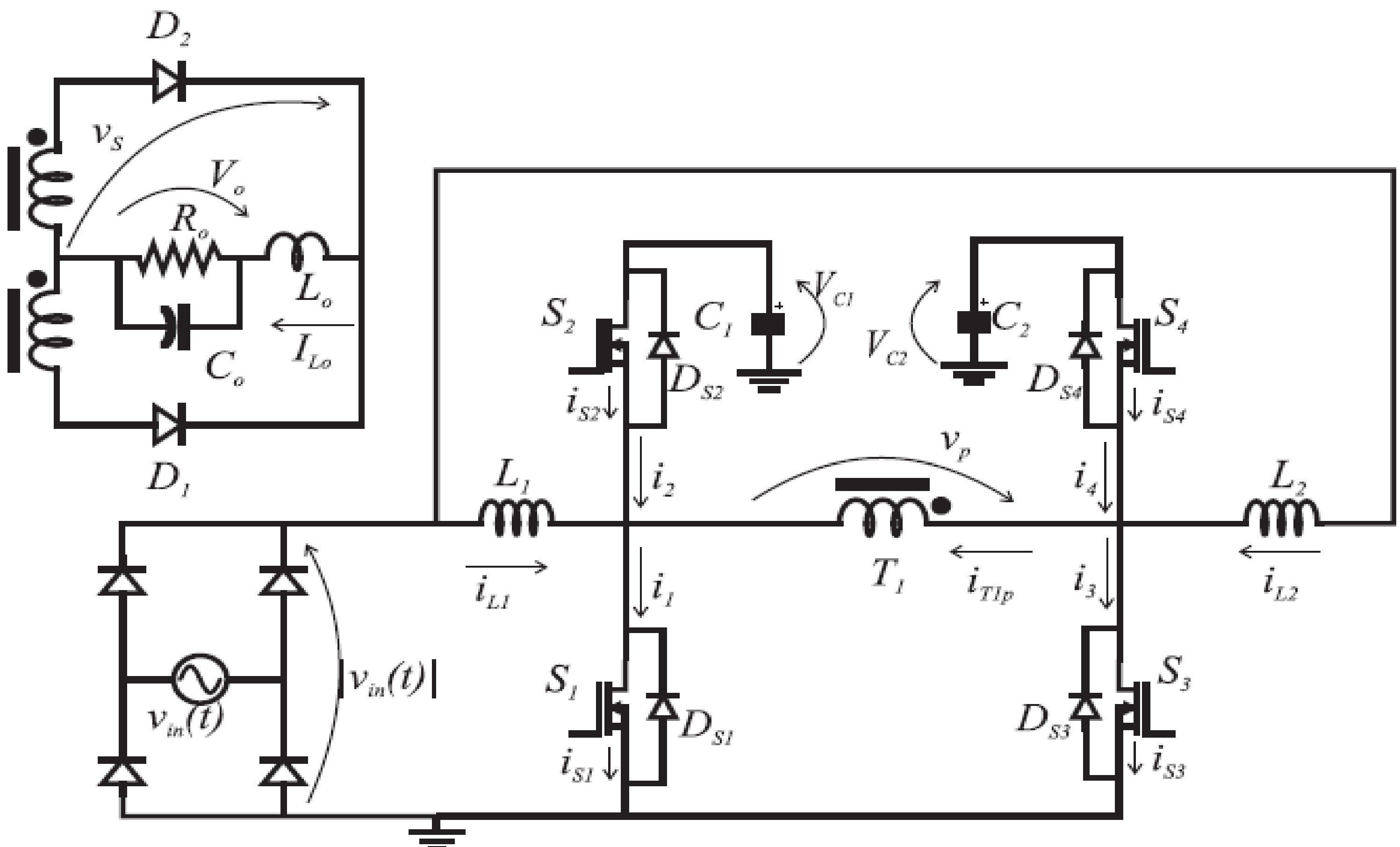


Figure 1. Topology proposed in

Interleaved Single-Stage AC-DC Converter [45] – Boost+ Flyback

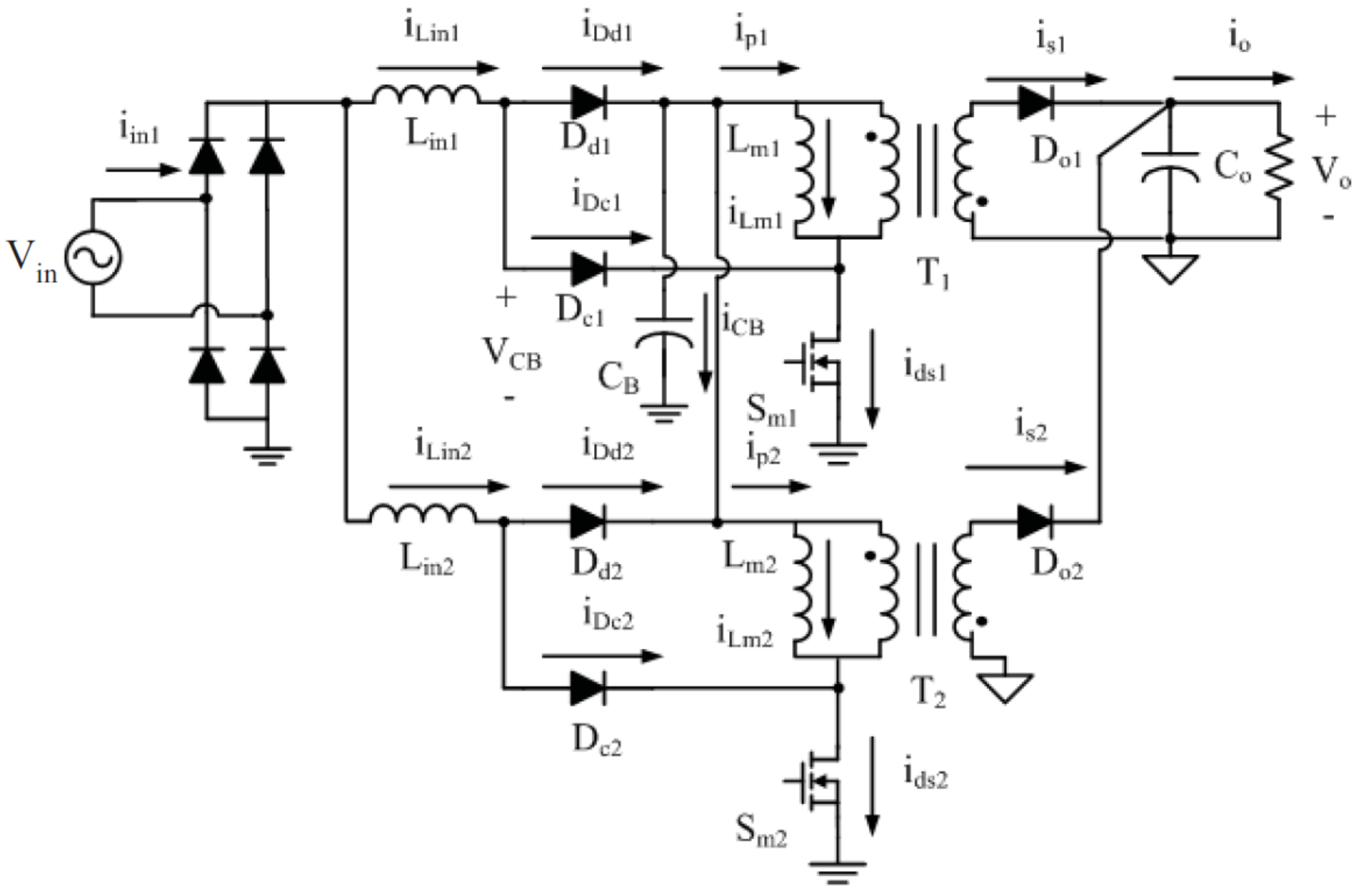


Fig. 2 circuit configuration of the proposed AC-DC boost-flyback converter.

Single-Stage PFC [46]

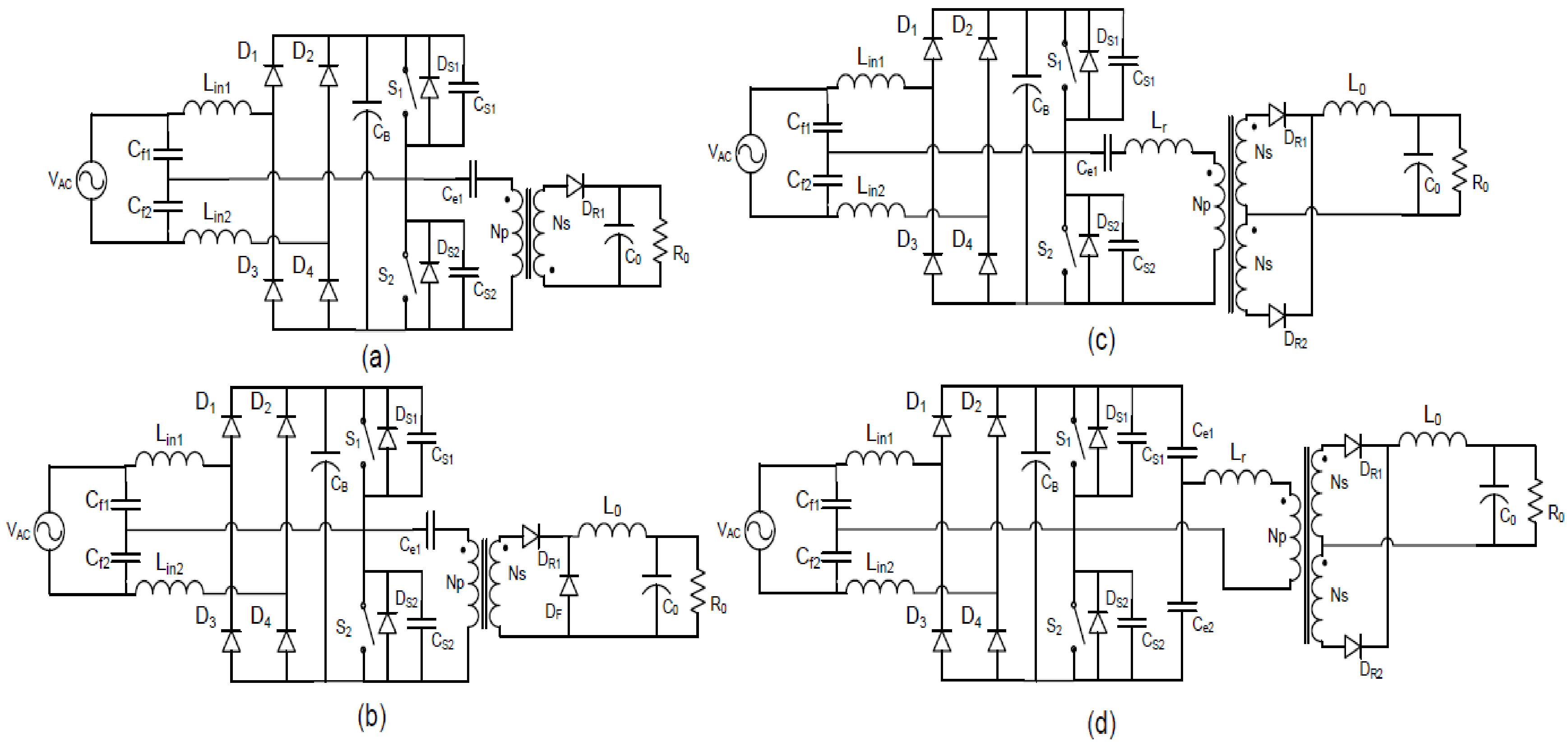


Figure 1. Proposed AC-DC converters: (a) PFC integrated with a flyback converter, (b) PFC integrated with a forward converter, (c) PFC integrated with an AHB converter, and (d) PFC integrated with a SHB converter.

Interleaved Single-Stage LLC Resonant Converter [47]

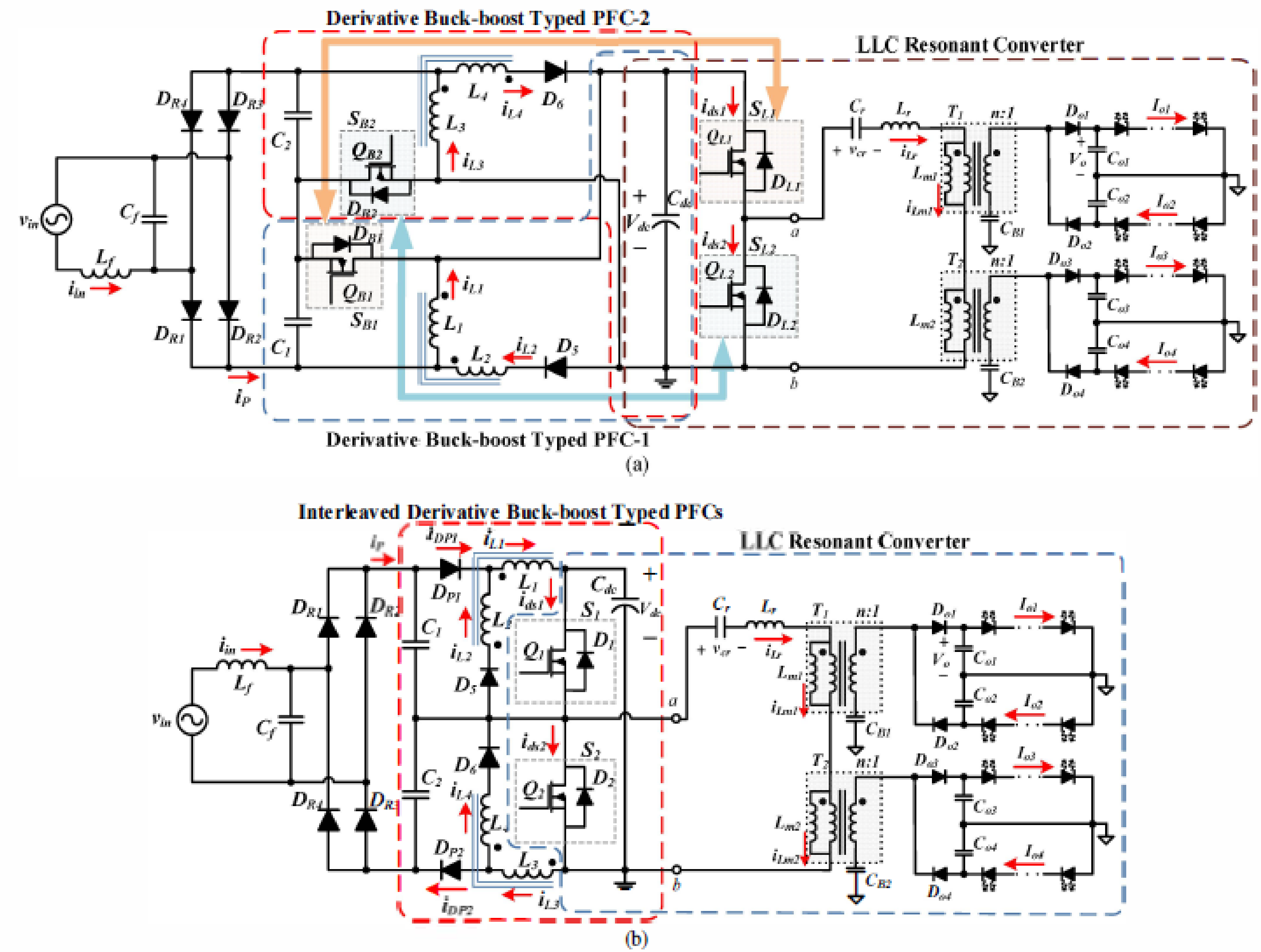


Fig. 3. Circuit derivation of the proposed single-stage LED driver.

➢ Discussion

A. Duality

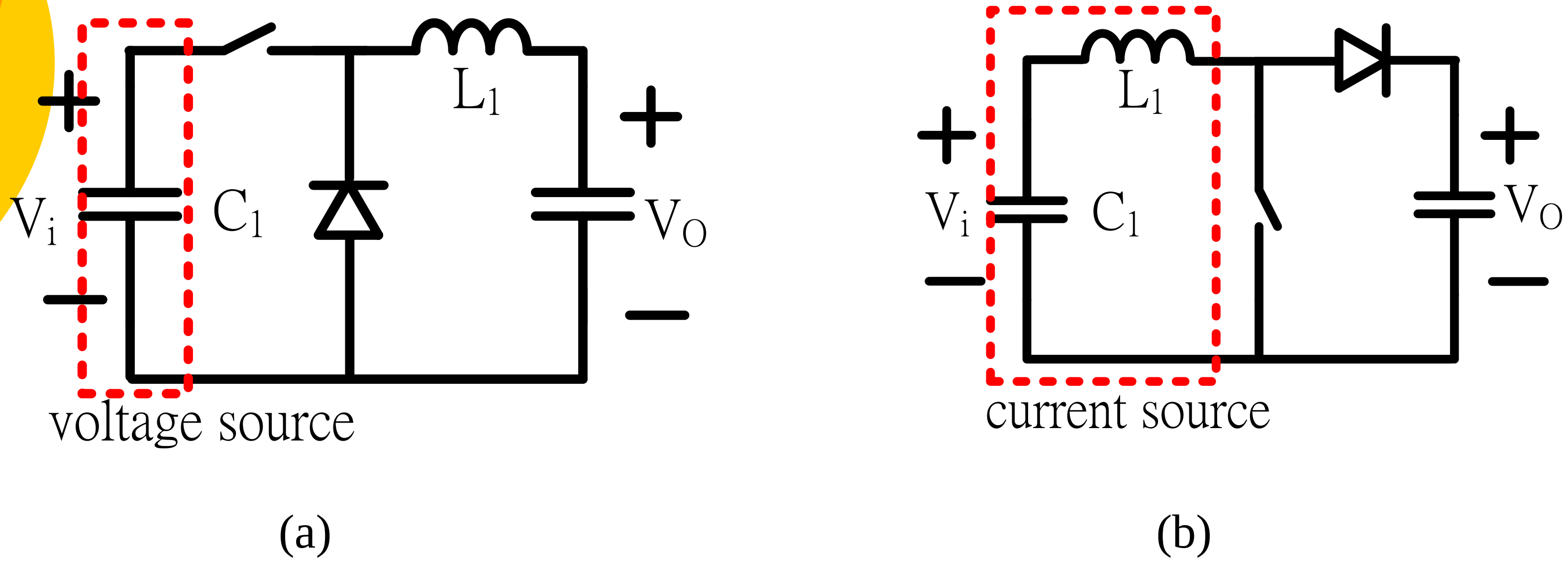


Fig. 30. Illustration of non-one-to-one correspondence of the duality between voltage source and current source.

What kind of dual is this?

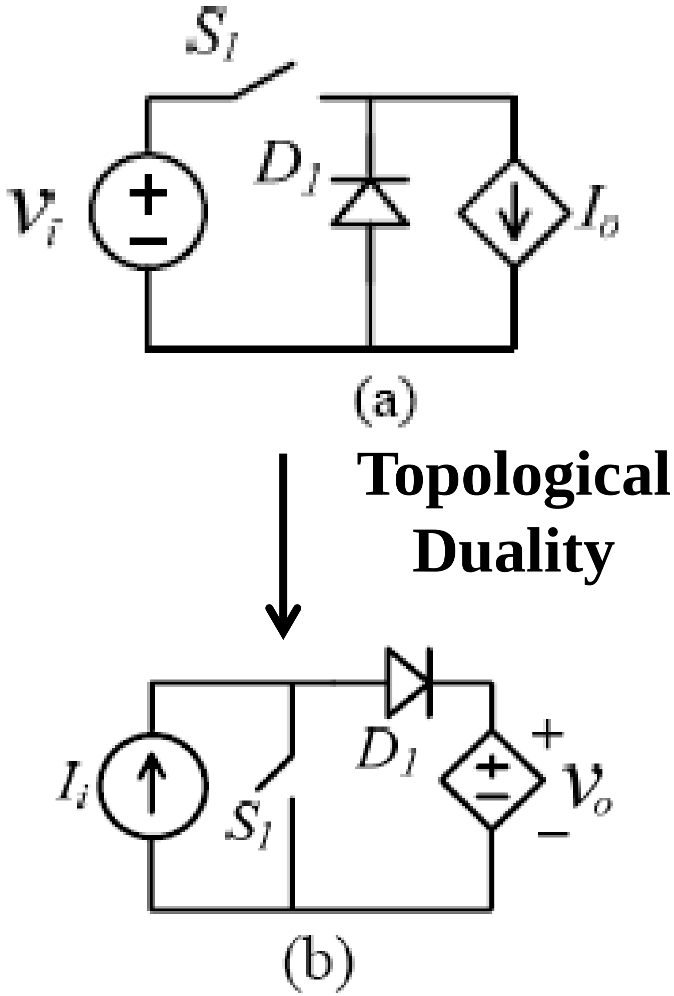


Fig. 31. (a) buck converter, and (b) boost converter in topological configuration

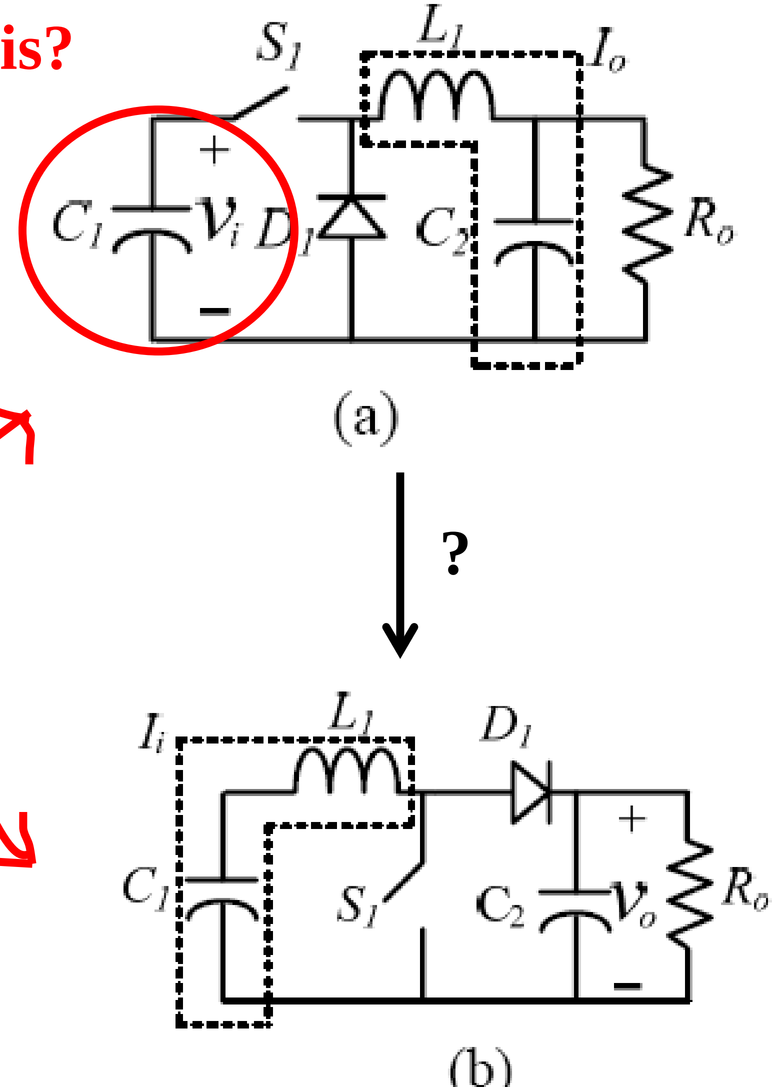


Fig. 32. (a) buck converter, and (b) boost converter in circuit configuration

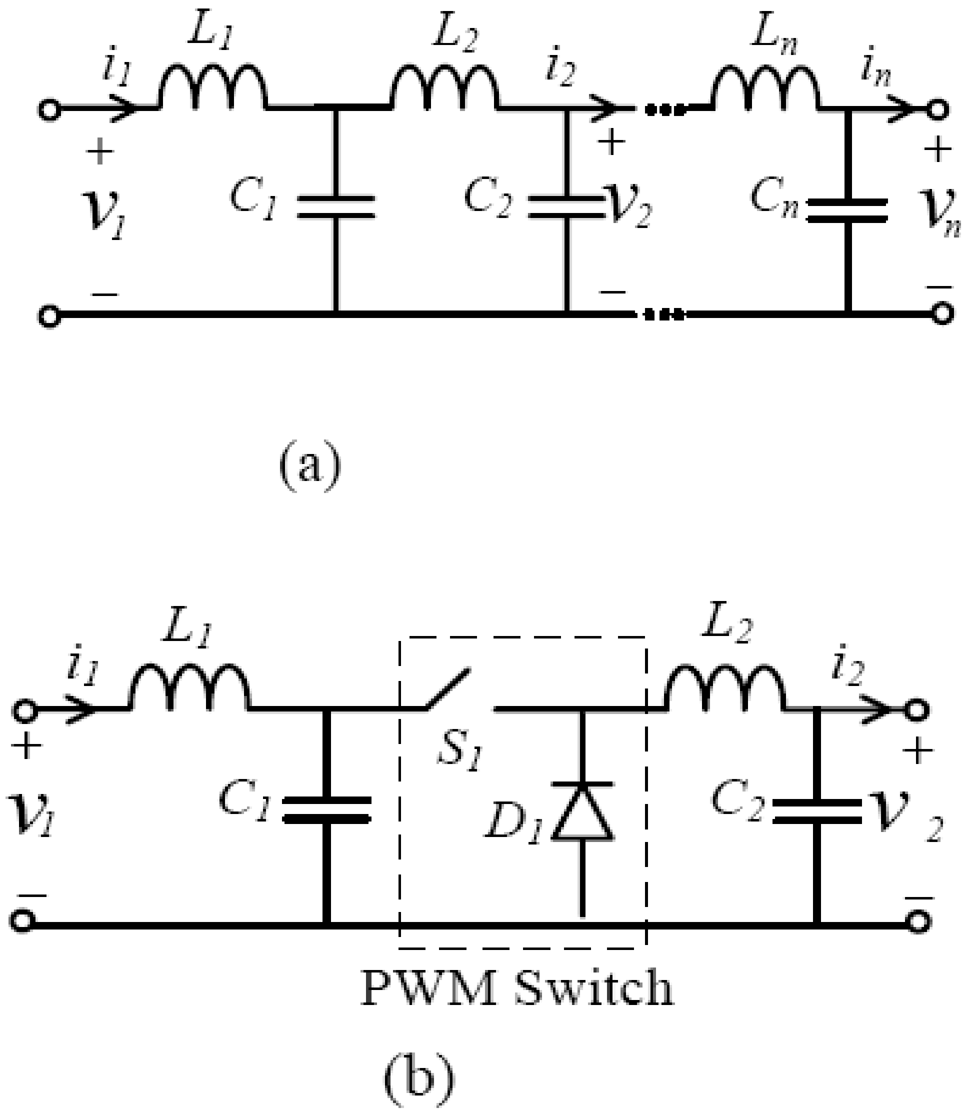
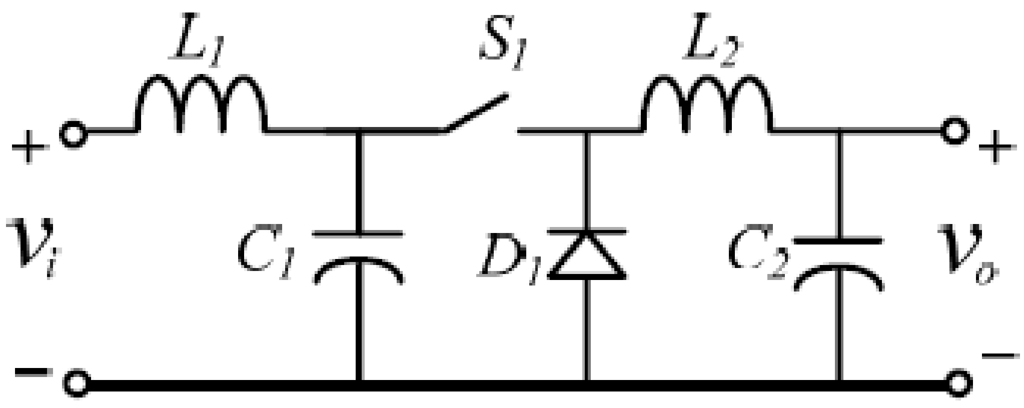
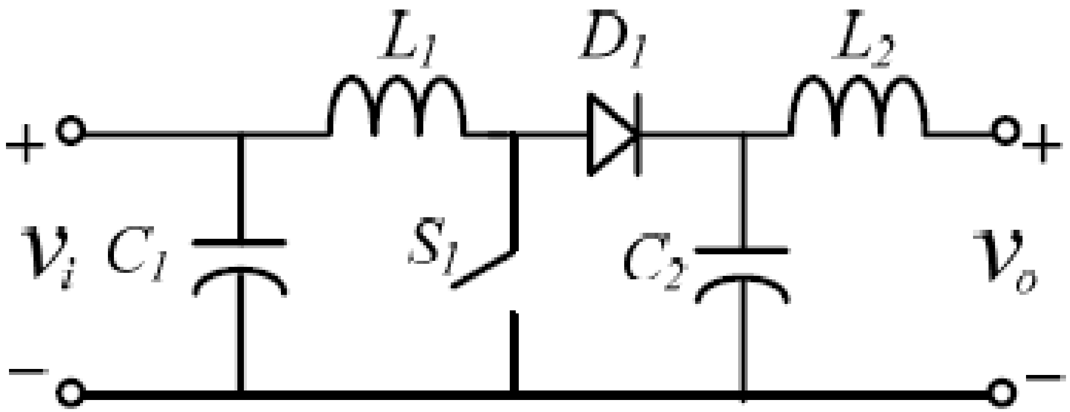


Fig. 33. (a) a transmission line modeled with L-C network

(b) a buck converter configured from resonance philosophy



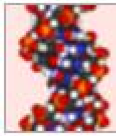
(a) Buck Converter



(b) Boost Converter

Fig. 34.

B. Analogy of PWM Converters to DNA



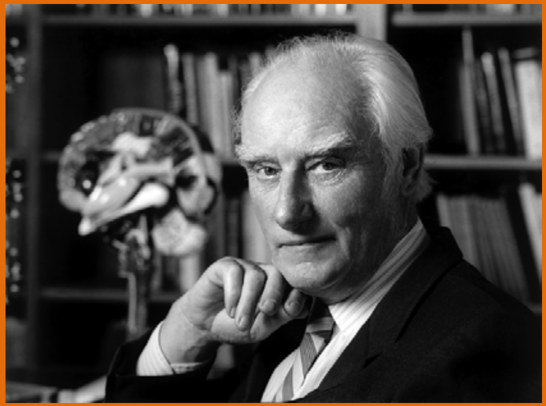
DNA雙螺旋結構發現人 1953年

佛朗西斯·克里克 | 羅莎琳·富蘭克林 | 雷蒙·葛斯林 | 艾力克·斯托克斯 | 莫里斯·威爾金斯 | 賀伯特·威爾森 | 詹姆斯·沃森

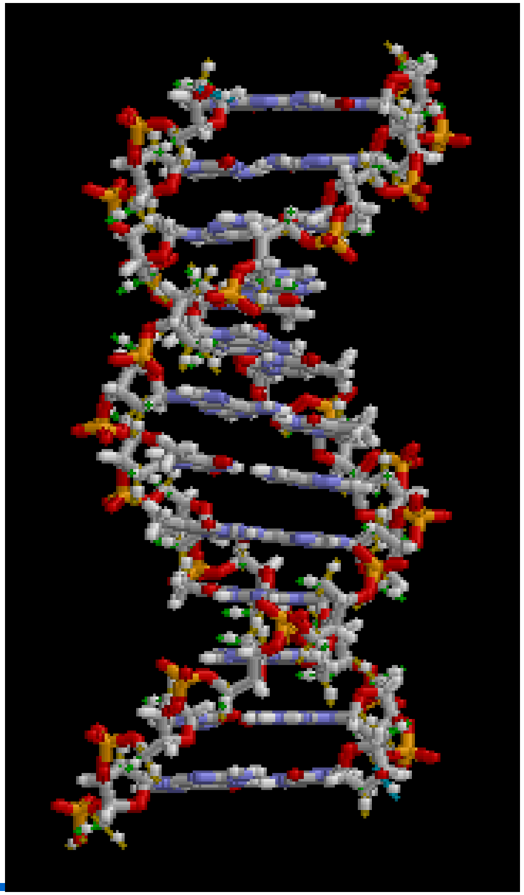
The Nobel Prize Winners in 1962.

James Dewey Watson

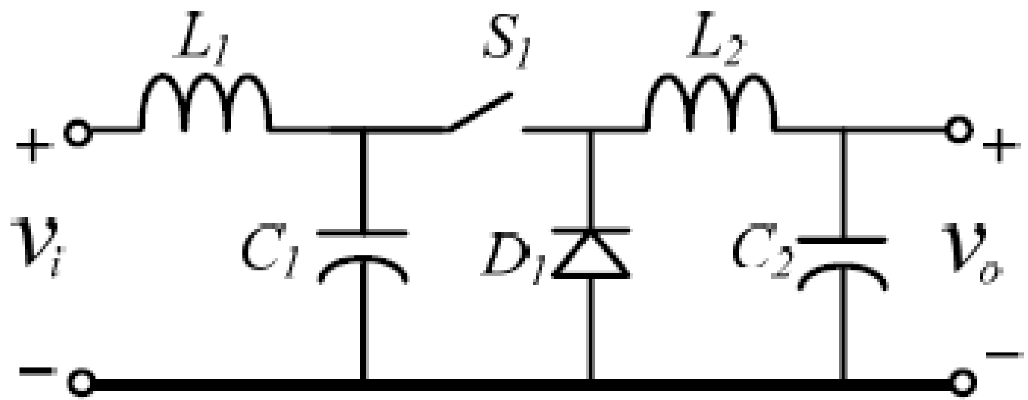
Maurice Hugh Frederick Wilkins



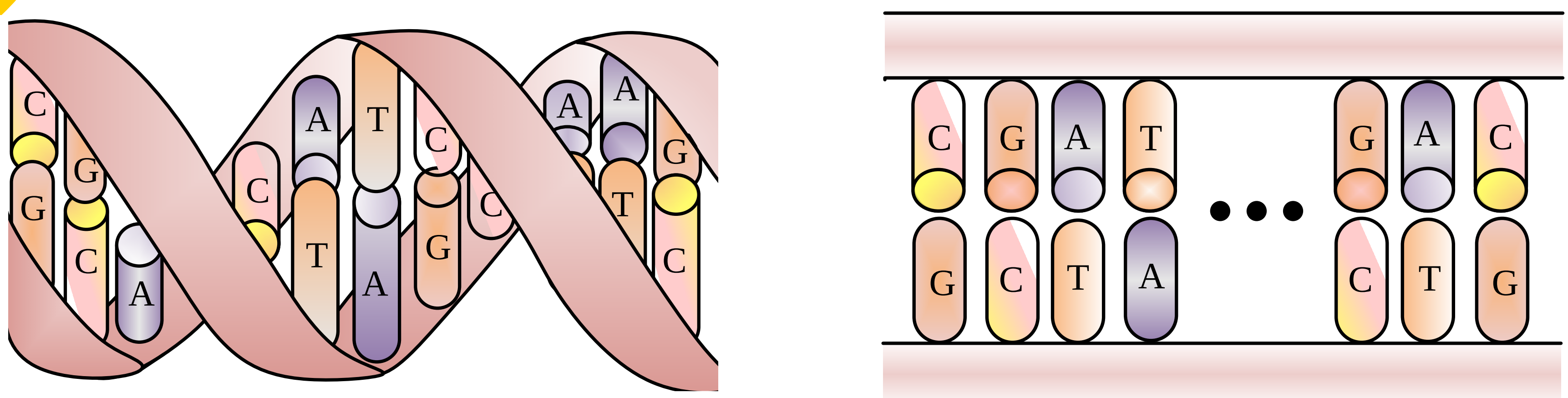
Francis Harry Compton Crick



資料來源：維基百科



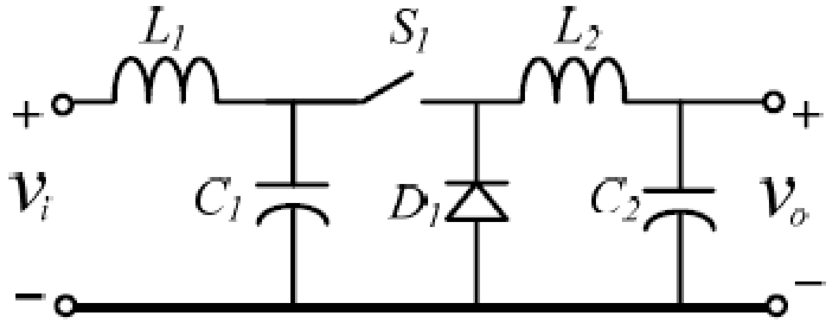
Two-port network



(a) (b)

Fig. 65. (a) DNA in double helix structure
(b) stretched DNA in two-port network like structure.

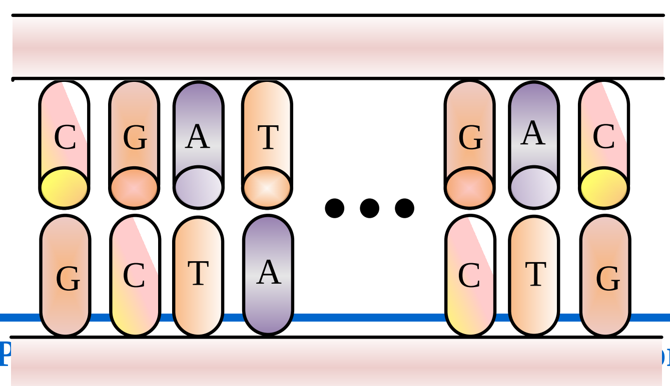
- **Converter ↔ DNA**



L, C, S, D ⟷ A(adenine), T(thymine), G(guanine), C(cytosine)

L ↔ C ⟷ A ↔ T

S ↔ D ⟷ G ↔ C



- **Converter ↔ DNA**

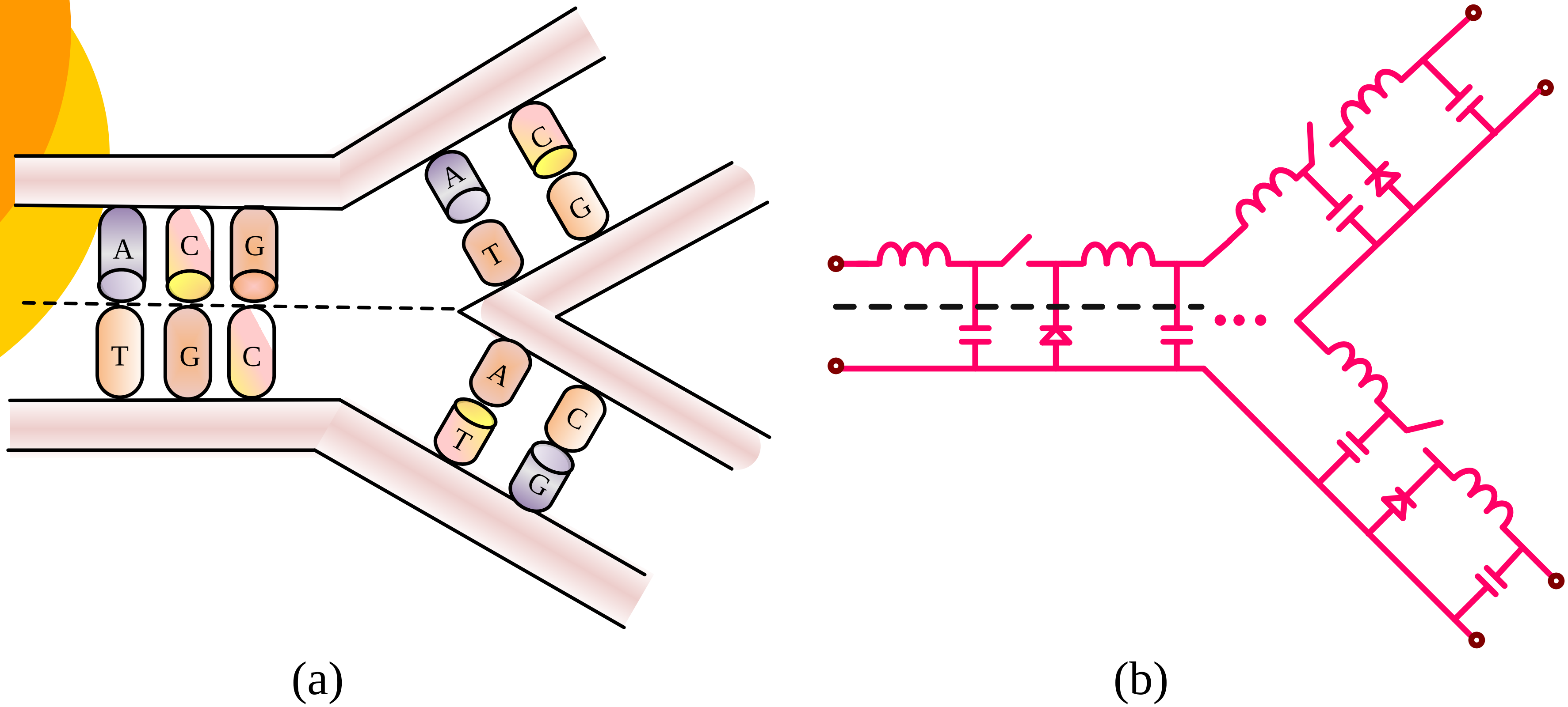


Fig. 35. Replication of (a) DNA and (b) PWM buck converter.

- **Converters**
  1. formed from codes L, C, S and D
  2. transfer power

- **DNA**
  1. formed from codes A, T, G and C
  2. transmit signal

跳脫本業窠臼 妙趣橫生

跨越領域鴻溝 海濶天空

馳騁學術疆場 創意無窮

究竟天下道理 萬源歸宗

1. Jumping out the trapped area, we will find a lot of fun.
2. Crossing the gap between fields, our mind can soar in the sky freely.
3. Based on this kind of mind, we can gallop free in academic field and have unlimited innovation.
4. After realizing the natural rules, we recognize that all of them just deduce from a simple principle.

Thanks for your attention

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