D-Σ Digital Control for Improving Stability Margin under High Line Impedance

Tsai-Fu Wu

Professor, National Tsing Hua University, Taiwan
Elegant Power Electronics Applied Research Laboratory (EPEARL)

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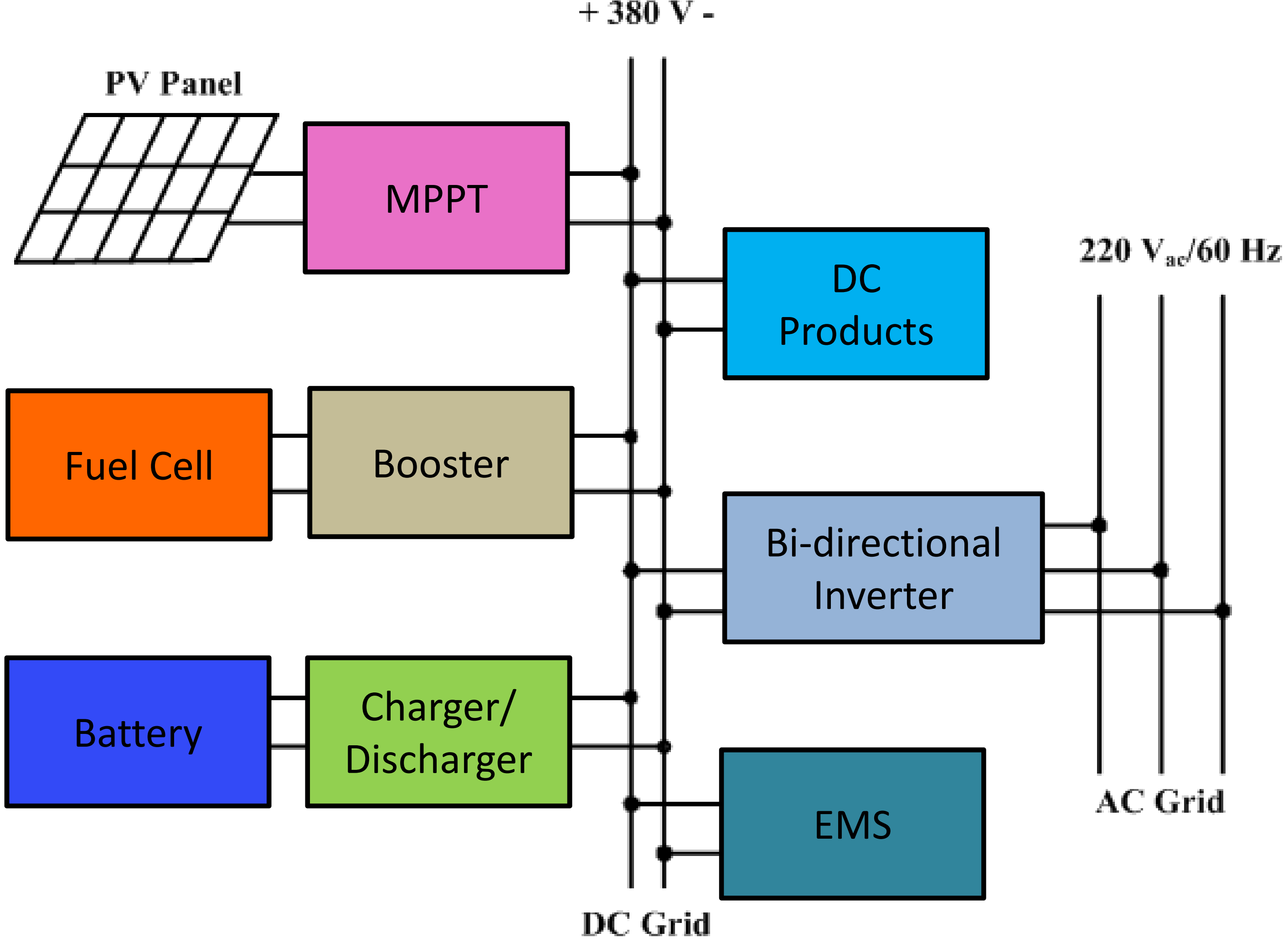
Outline

- # Introduction
- # D-Σ Digital Control
- # Filter-Capacitor Current Compensation
- # Stability Analysis
- # Experimental Results
- # Conclusions

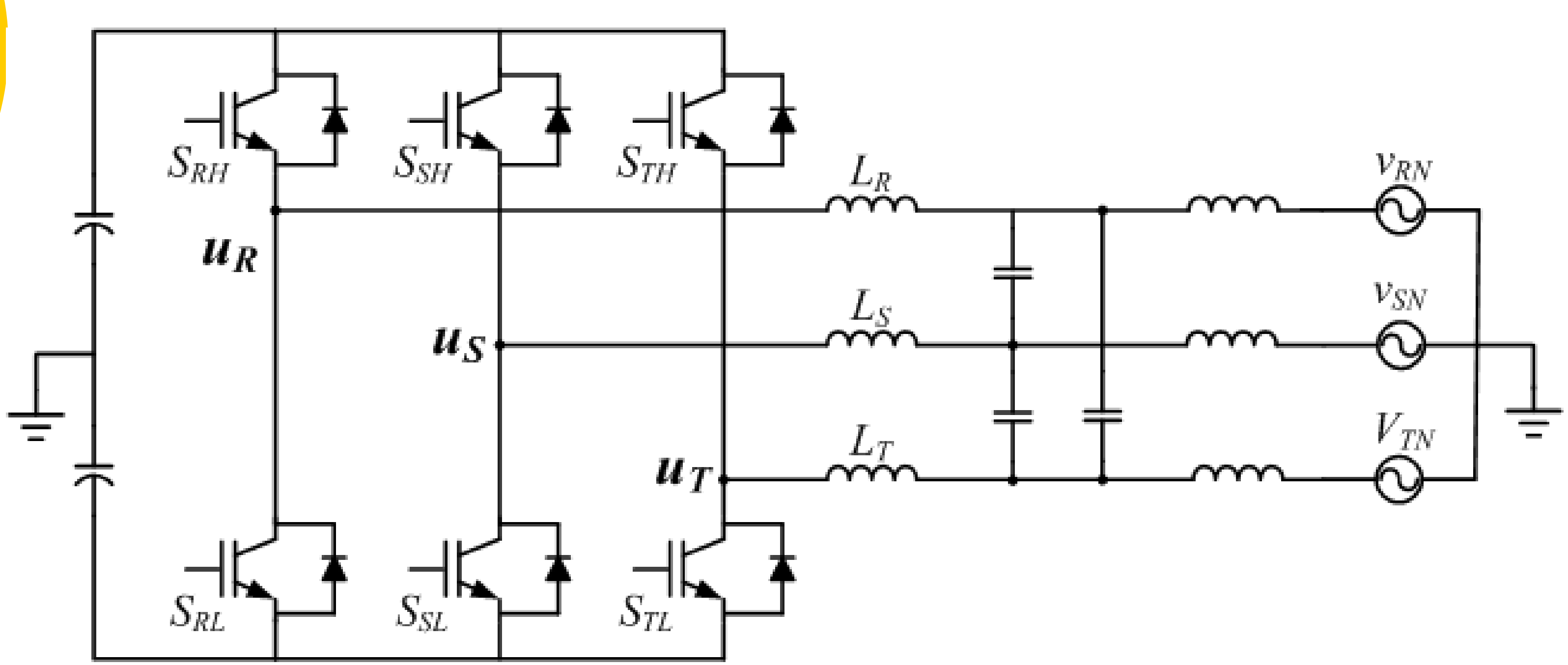
Introduction

➢ Harmonized AC and DC Microgrid

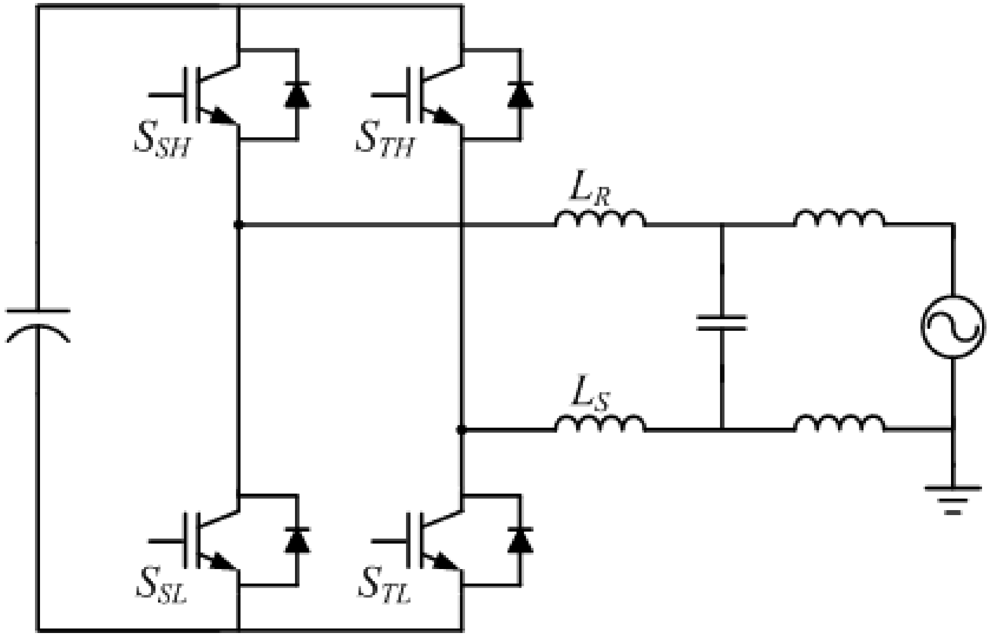


Bi-directional Inverter

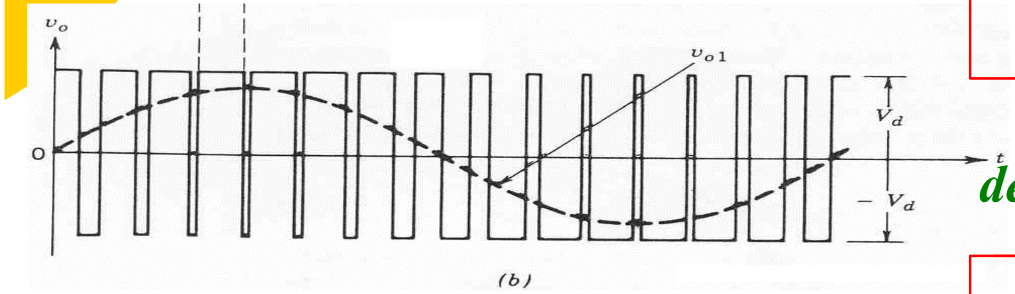
- 3Φ4W Inverter (= 3 x 1 Φ 2W Inverters)



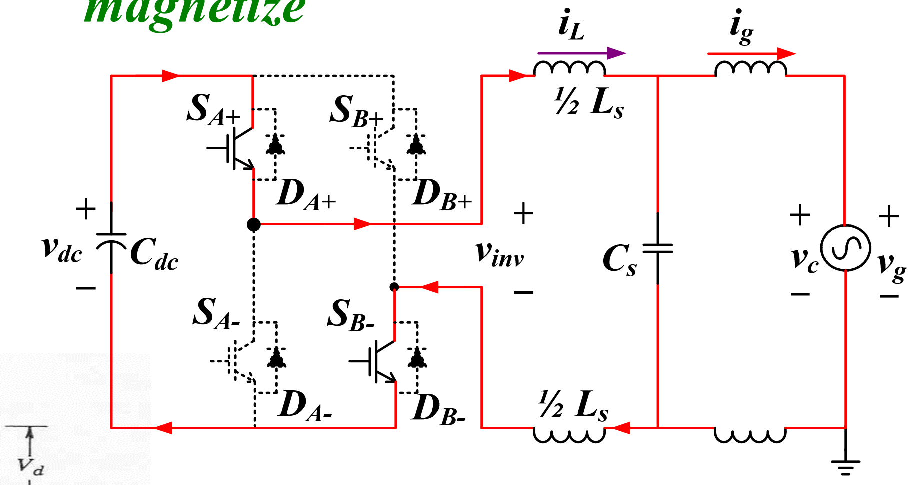
- **1Φ2W Inverter**



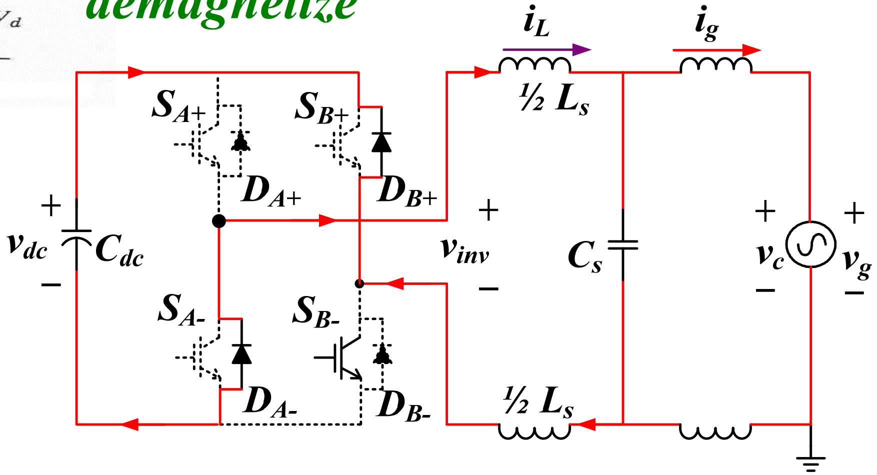
➢ SPWM and Bi-Polar Operation



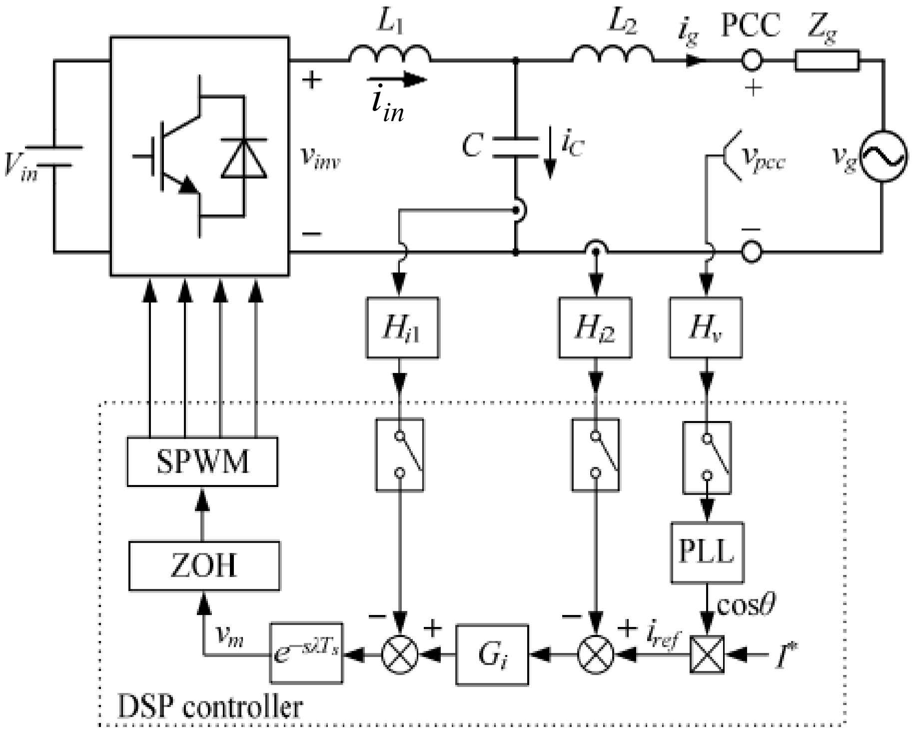
magnetize



demagnetize



- **Conventional Approach**

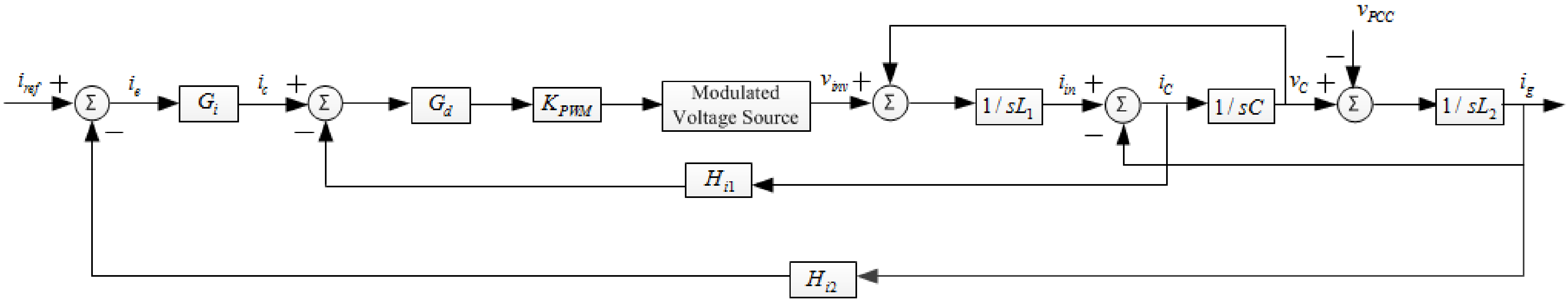


where:

$$G_i = K_P + \frac{K_i}{s}$$

$$G_d \approx e^{-s(\lambda+0.5)T_s} \quad (0 \le \lambda \le 1)$$

$$K_{PWM} = \frac{V_{in}}{V_{tri}}$$



D-Σ Digital Control

➢ Major Characteristics

1) No need of frame transformation (for three-phase systems), the D-Σ digital control determining control laws directly.

2) Unlike predictive control, the D-Σ digital control using all of the information known *a priori*.

3) Similar to deadbeat control, the D-Σ digital control determining control law directly without modulation.

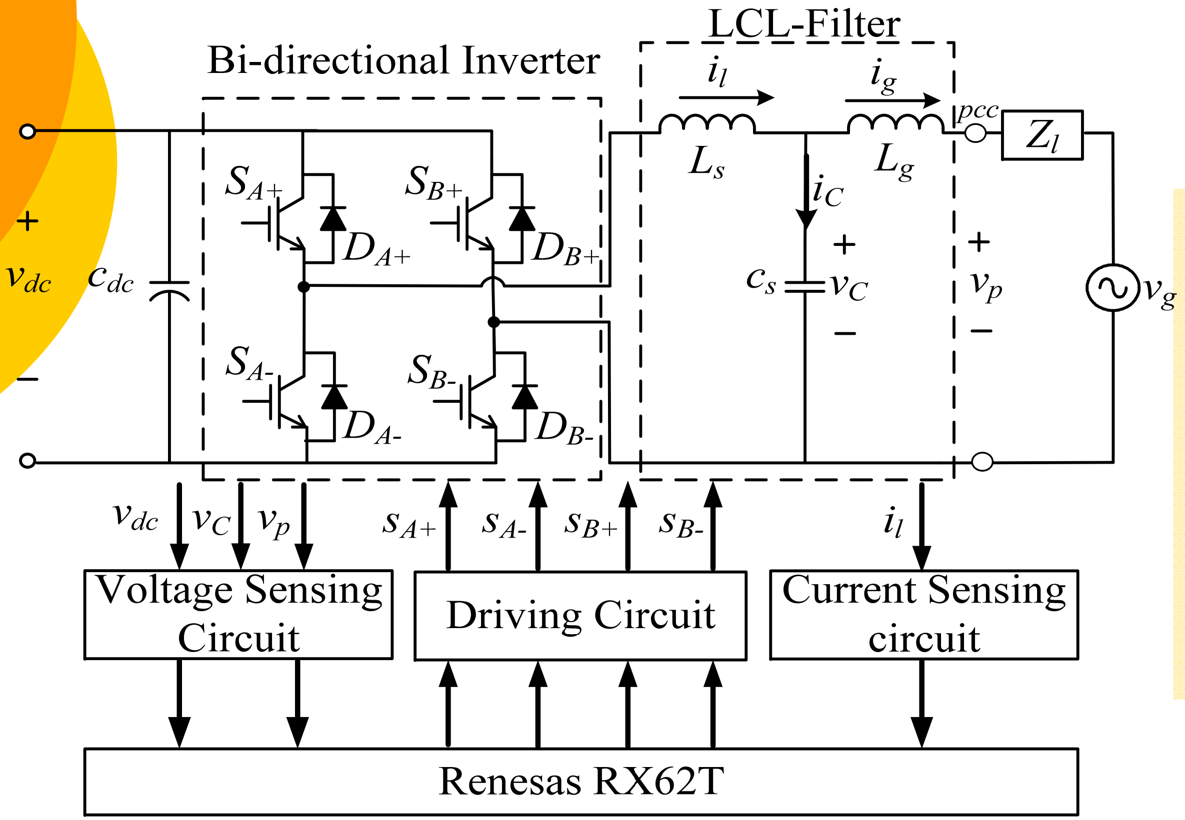
4) Unlike deadbeat control, the D-Σ digital control having a controller to cover wide filter inductance, dc-bus voltage and switching frequency variations.

5) Like fuzzy control, the D-Σ digital control being named based on the processes of control-law derivation.

➢ Unique Features

1) Direct digital control -- link error to control directly.
2) Current source – achieve high stability margin.
3) $G_C \bullet G_P = I$ – cancel parameter variation effects.
4) Wide bandwidth – up to switching frequency.

Single-Phase Bi-directional Inverter



- D-Σ digital control
- Cover wide inductance variation and grid voltage distortion.
- Shape grid-current sinusoidally.
- Achieve wide BW (= f_s).

Circuit diagram of a single-phase bi-directional inverter with LCL filter and its control blocks.

Derivation of Control Laws

A. Grid-Connection Mode

Two buck converters operated in +tive and –tive half line cycles, respectively.

B. Rectification Mode

Two boost converters operated in +tive and -tive half line cycles, respectively.

D- Σ Approach (Grid –Connection Mode)

Division (D) of Switching Period:

$$\Delta i_{Ls,magnetize} = \frac{v_{dc} - v_c}{L_s(i_l)} dT_s$$

+) and

$$\Delta i_{Ls,demagnetize} = -\frac{v_{dc} + v_c}{L_s(i_l)} (1-d)T_s$$

$$\Delta i_L = \frac{v_{dc} - v_c}{L_s(i_l)} dT_s - \frac{v_{dc} + v_c}{L_s(i_l)} (1-d)T_s$$

Summation: Σ

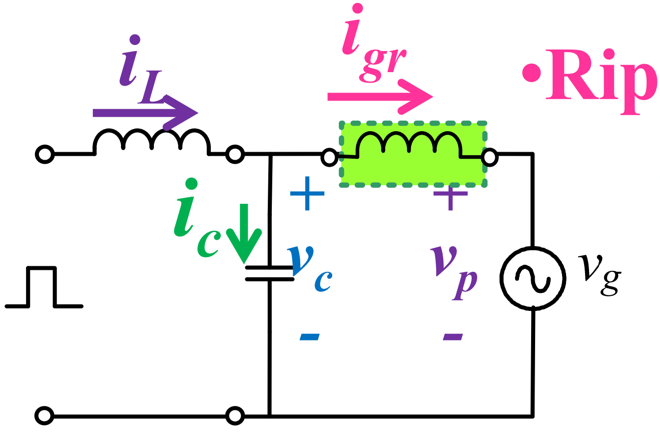
Control law for grid-connection mode:

$$d_{GC} = \frac{1}{2} + \frac{v_c}{2v_{dc}} + \frac{\Delta i_L \cdot L_s(i_l)}{2v_{dc} \cdot T_s}$$

Control law for rectification mode:

$$d_{\text{Rec}} = 1 - d_{GC} = \frac{1}{2} - \frac{v_c}{2v_{dc}} - \frac{\Delta i_L \cdot L_s(i_l)}{2v_{dc} \cdot T_s}$$

LC or LCL Filter



LC filter network at the inverter output side.

•Ripple Current

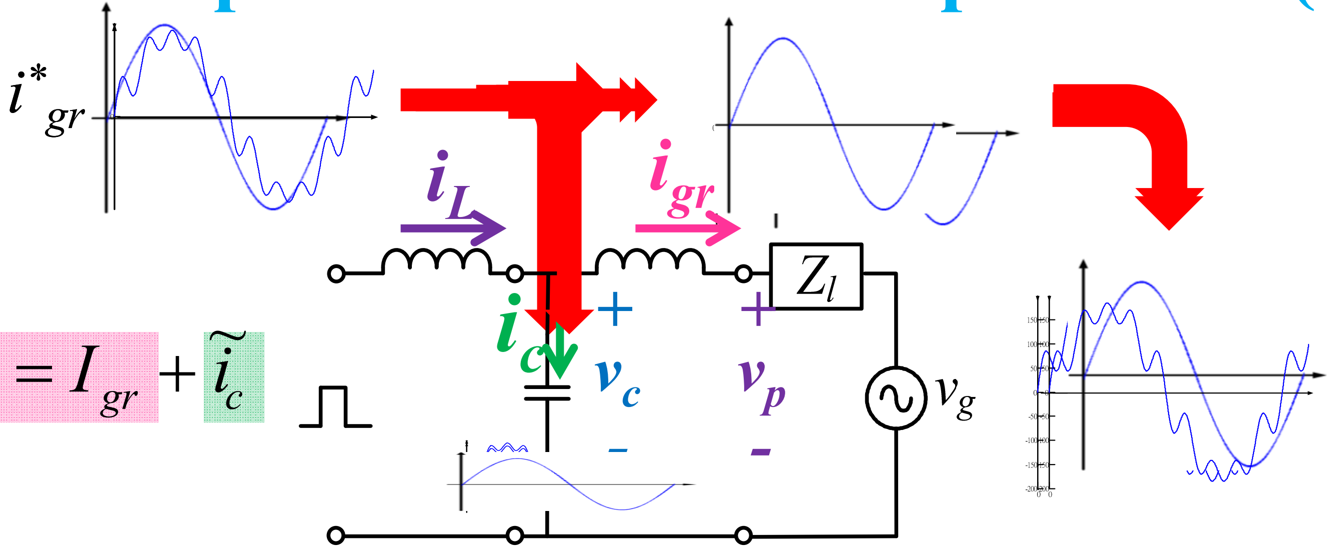
✓ LCL Filter

$$d_{GC} = \frac{1}{2} + \frac{v_c}{2v_{dc}} + \frac{\Delta i_L(n+1) \cdot L_s(i_L)}{2v_{dc} \cdot T_s}$$

$$\Delta i_L(n+1) = I_{gr}(n+1) - i_{Lfb}(n)$$
$$= (I_{gr}(n) - i_{Lfb}(n)) + (I_{gr}(n+1) - I_{gr}(n))$$

$$I_{gr} = I_M \sin(n\omega T_S)$$

Filter-Capacitor Current Compensation (FCCC)



$$i^*_{gr} = I_{gr} + \tilde{i}_c$$

LCL filter network at the inverter output side.

$$d_{GC} = \frac{1}{2} + \frac{v_c}{2v_{dc}} + \frac{\Delta i_L(n+1)\cdot L_s(i_L)}{2v_{dc}\cdot T_s}$$

$$\Delta i_L(n+1) = I_{gr}(n+1) - i_{Lfb}(n)$$

$$I_{gr} = I_M \sin\left(n\omega T_S\right)$$

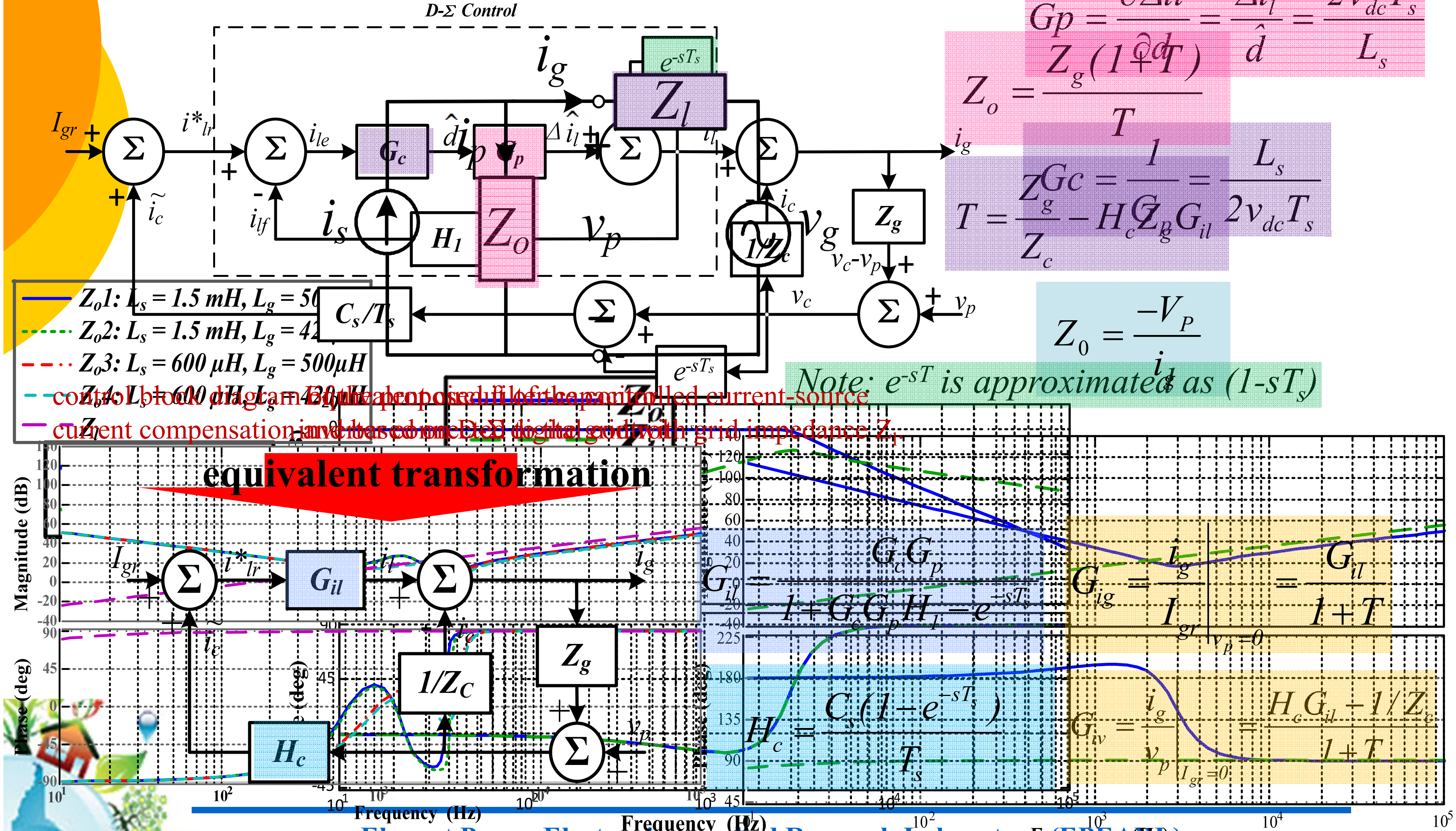
$$\Delta i_L(n+1) = i^*_{gr}(n+1) - i_{Lfb}(n)$$

$$\tilde{i}_c = \frac{C_s\left(\tilde{v}_c(n+1) - v_c(n)\right)}{T_s}$$

$$\tilde{v}_c(n+1) = v_p(n) + \frac{L_g(I_{gr}(n+1) - I_{gr}(n-1))}{T_S}$$

Stability Analysis

➢ s-domain model



control block diagram of the proposed controlled current-source current compensation inverter based on D-Σ digital control

[illegible] of the [illegible] filter capacitor [illegible] connected to the grid with grid impedance Z_l.

$$Gp = \frac{\partial \Delta il}{\partial d} = \frac{\Delta \hat{i}_l}{\hat{d}} = \frac{2v_{dc}T_s}{L_s}$$

$$Z_o = \frac{Z_g(1+T)}{T}$$

$$Gc = \frac{1}{G_p} = \frac{L_s}{2v_{dc}T_s}$$

$$T = \frac{Z_g}{Z_c} - H_c Z_g G_{il}$$

$$Z_0 = \frac{-V_P}{i_l}$$

Note: e^{-sT} is approximated as $(1-sT_s)$

$$G_{il} = \frac{G_cG_p}{1+G_cG_pH_1-e^{-sT_s}}$$

$$H_c = \frac{C_s(1-e^{-sT_s})}{T_s}$$

$$G_{ig} = \left.\frac{i_g}{I_{gr}}\right|_{v_p=0} = \frac{G_{il}}{1+T}$$

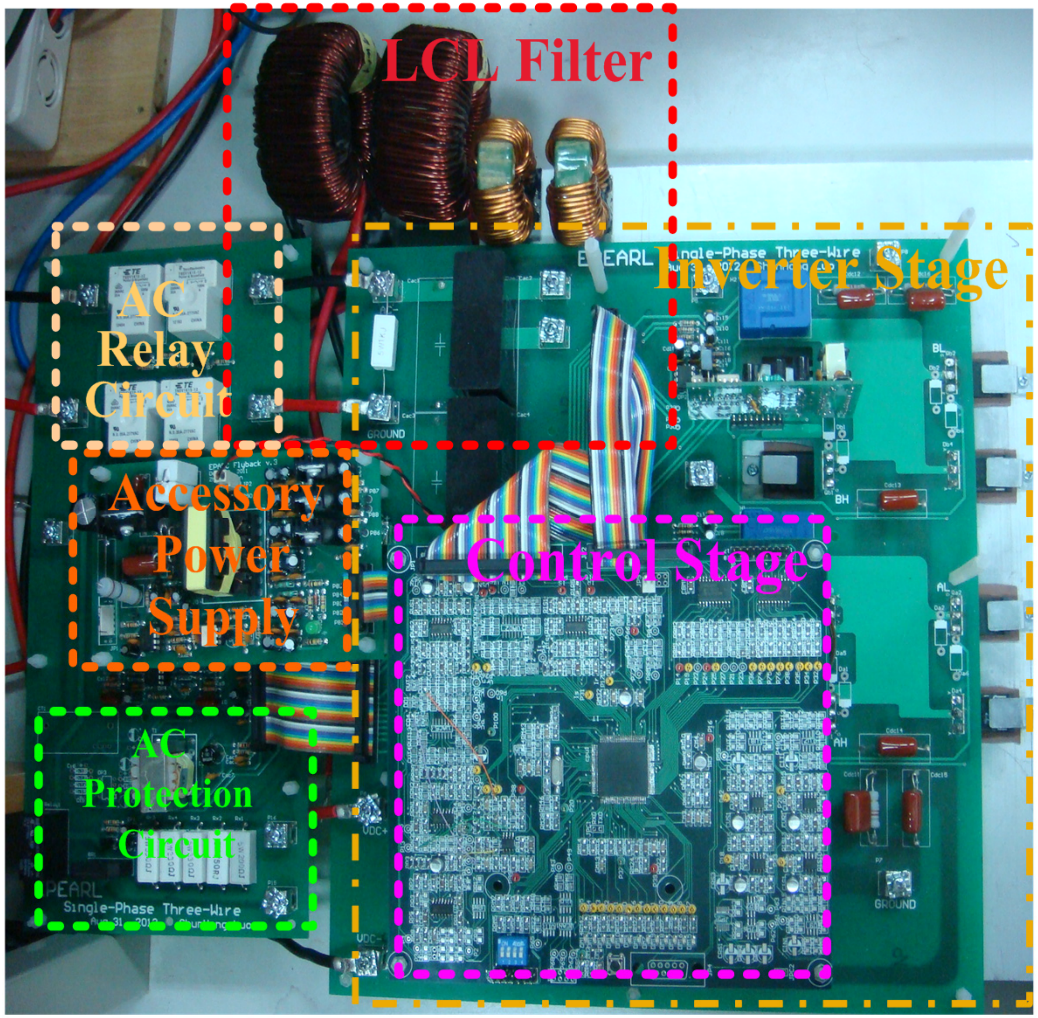
$$G_{iv} = \left.\frac{i_g}{v_p}\right|_{I_{gr}=0} = \frac{H_cG_{il}-1/Z_c}{1+T}$$

Specifications

SYSTEM PARAMETERS OF THE EXPERIMENT SET-UP

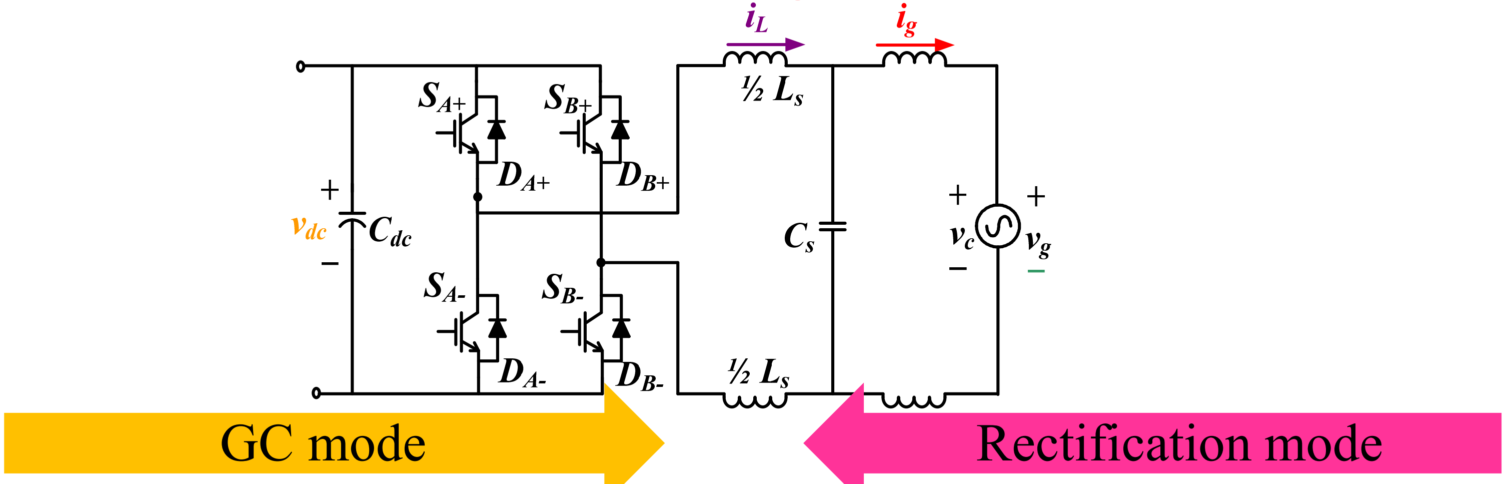
Parameters	Symbols	Values
DC-bus voltage	v_{DC}	360 ~ 400 V
AC output voltage	v_N	220 V_{rms}
Maximum rated power	P_{max}	5 kW
Line frequency	f_l	60 Hz
Inverter inductors	L_s	3 mH ~ 650 μH
Filter capacitor	C_s	5 μF
Power switch	IGBT IRG4PC50SPbF	$V_{CE(on)\ typ.}$ = 1.28 V, V_{CES} = 600V, and $I_{C(TC=25^\circ C)}$ = 70 A
Power diode (silicon carbide)	CREE C3D20060D	$V_{F(TJ=25^\circ C)\ typ.}$ = 1.5 V Zero-Recovery Time
Switching frequency	f_s	20 kHz

- **Prototype**

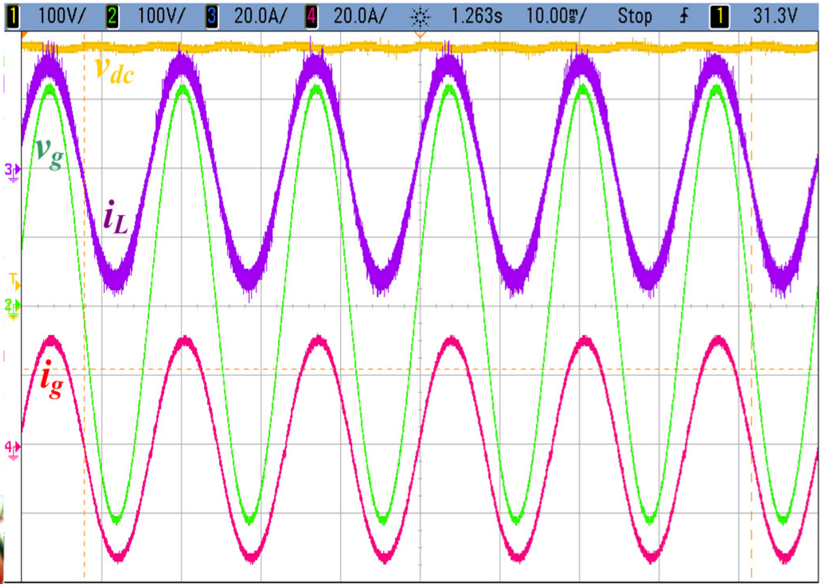


Photograph of the designed single-phase bi-directional inverter system

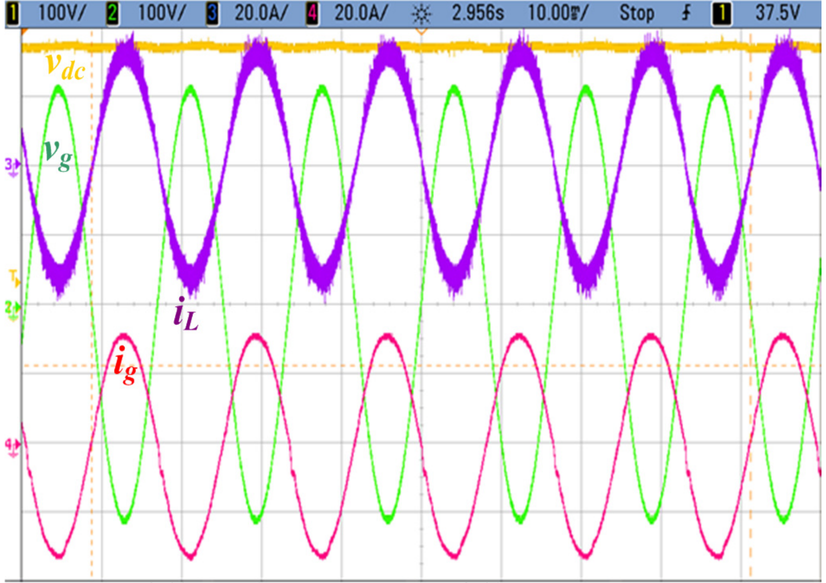
Experimental Results (Vg with no harmonics)



GC mode (5 kW)

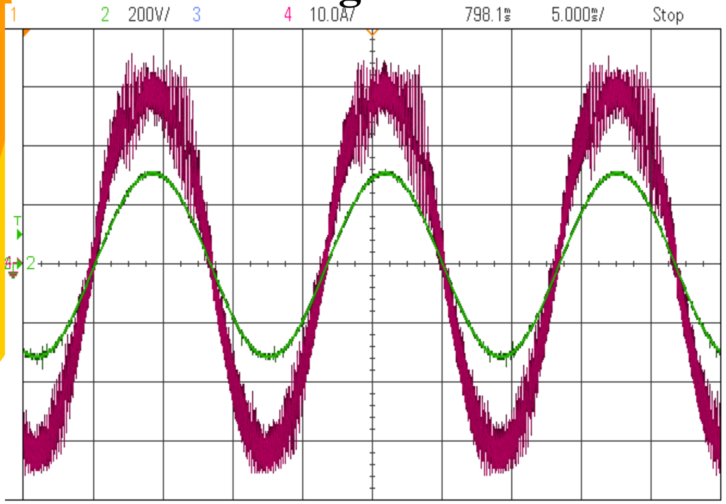


Rectification mode (5 kW)

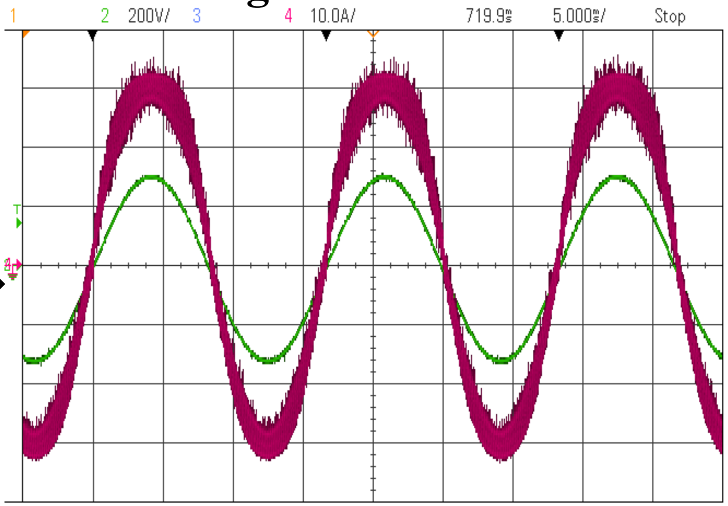


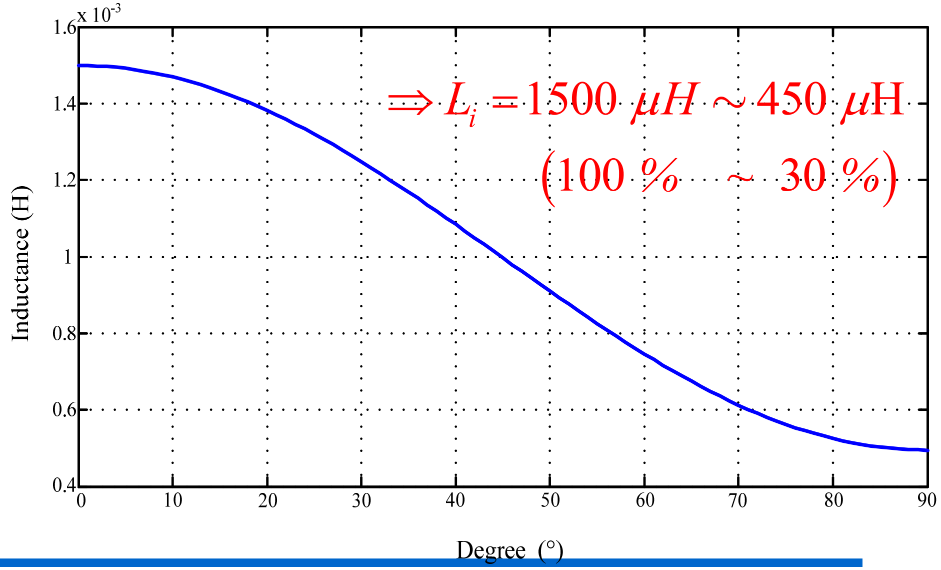
(i_L *and* i_g: 20A/div; v_g *and* v_{dc}: 100v/div; time: 10ms/div)

Without considering inductance variation



Considering inductance variation

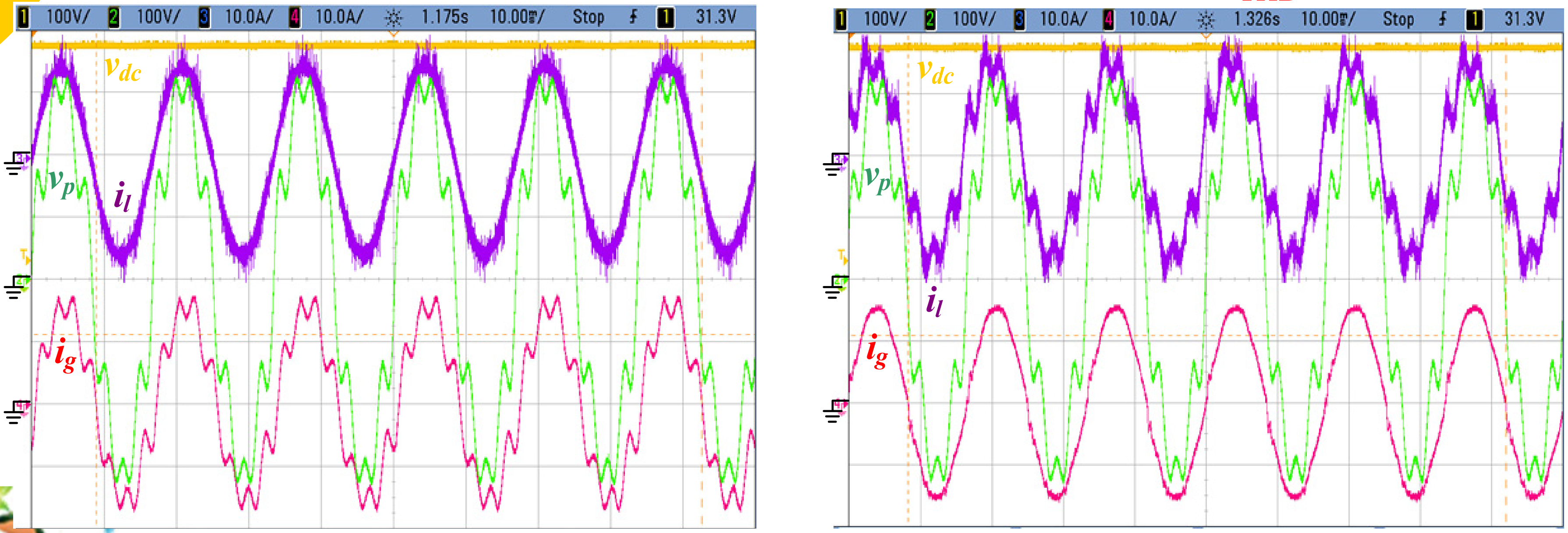




➢ Experimental Results (GC mode) (V_g with harmonics)

✓ ***Case I:*** (V_{THD} : 18.5%)

Harmonic order	%
5	9.8
7	15.8
8	2.16



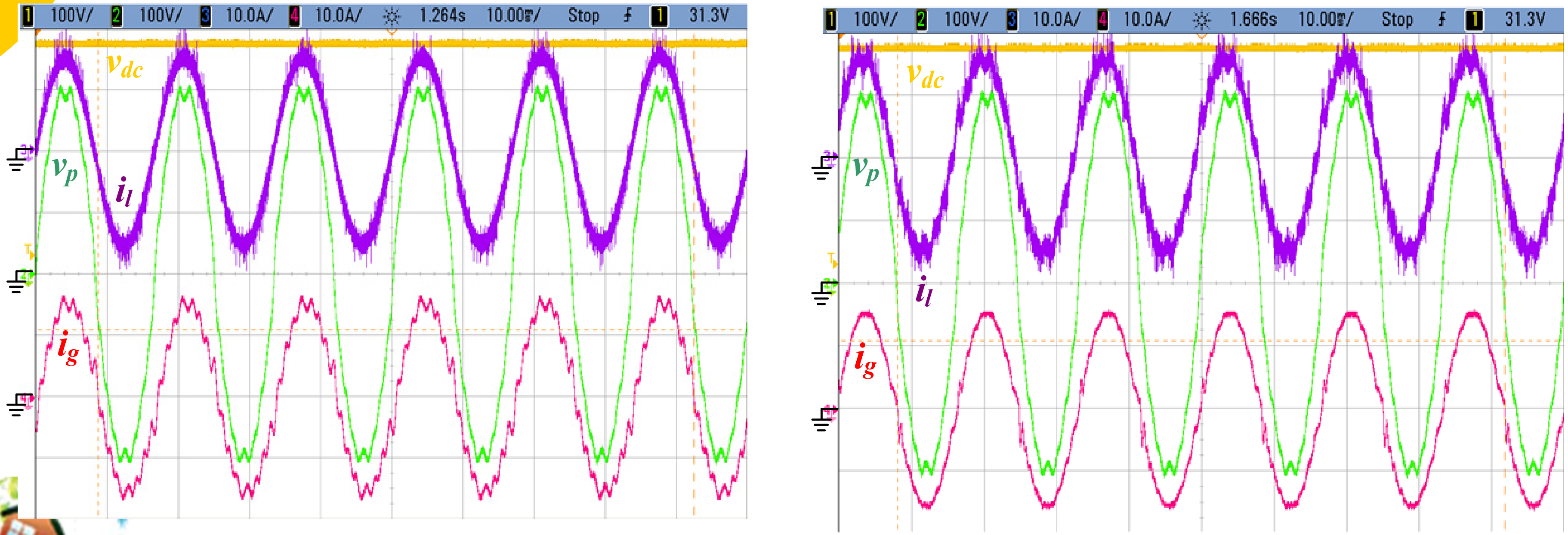
Without FCCC I_{THD}: 18.8%

With FCCC I_{THD}: 3.2%

(i_L *and* i_g: 10A/div; v_g *and* v_{dc}: 100v/div; time: 10ms/div)

- ✓ ***Case II:*** (V_{THD} : 6.4%)

Harmonic order	%	Harmonic order	%
3	4.9	11	1.4
5	1.6	15	2
7	2.7	17	1.1

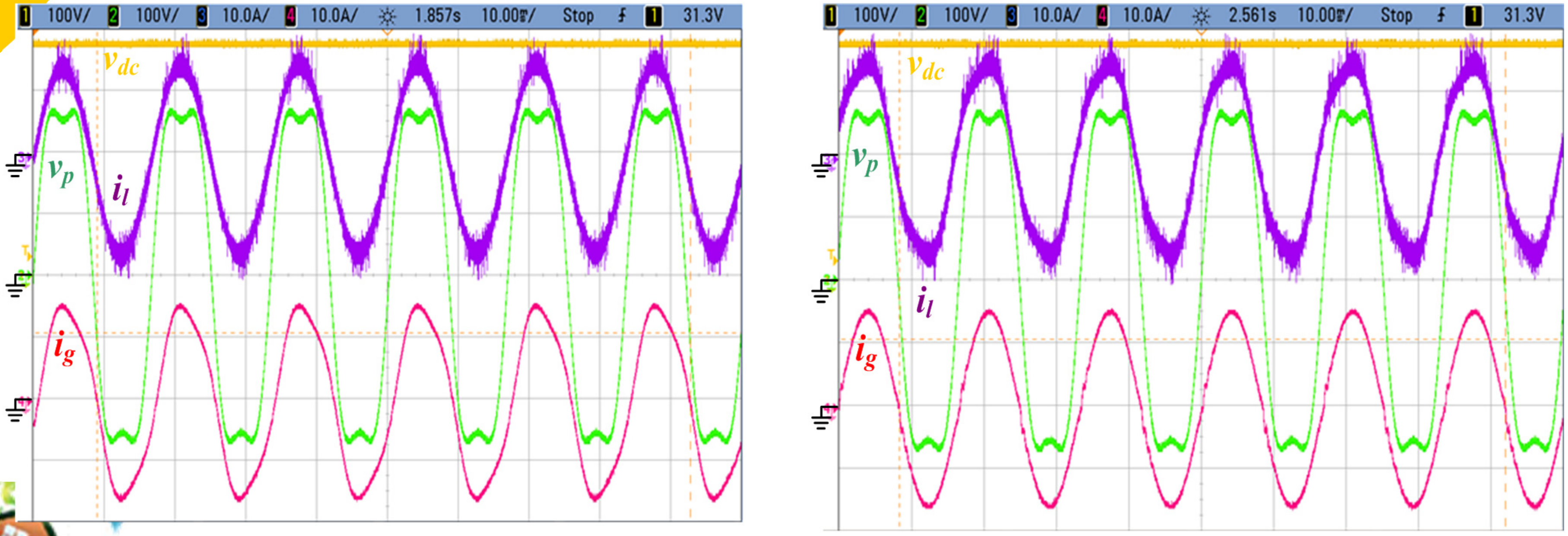

Without FCCC I_{THD}: 9.4%

With FCCC I_{THD}: 3.8%

(i_L *and* i_g: 10A/div; v_g *and* v_{dc}: 100v/div; time: 10ms/div)

- ✓ ***Case III:*** (V_{THD} : 17.8%)

Harmonic order	%
3	17.8



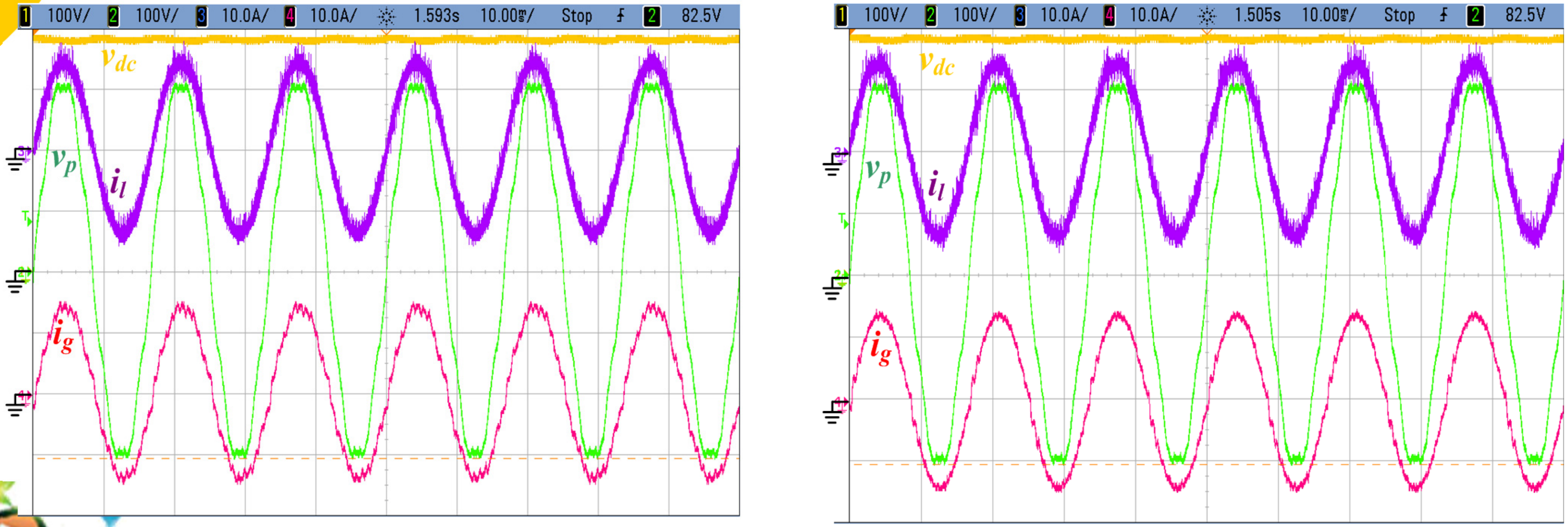
Without FCCC I_{THD}: 17.7%

With FCCC I_{THD} : 2.1%

(i_L *and* i_g: 10A/div; v_g *and* v_{dc}: 100v/div; time: 10ms/div)

- ✓ ***Case IV:*** (V_{THD} : 4.9%)

Harmonic order	%	Harmonic order	%
7	4.6	21	0.9
9	1	39	0.7



Without FCCC I_{THD}: 5.1%

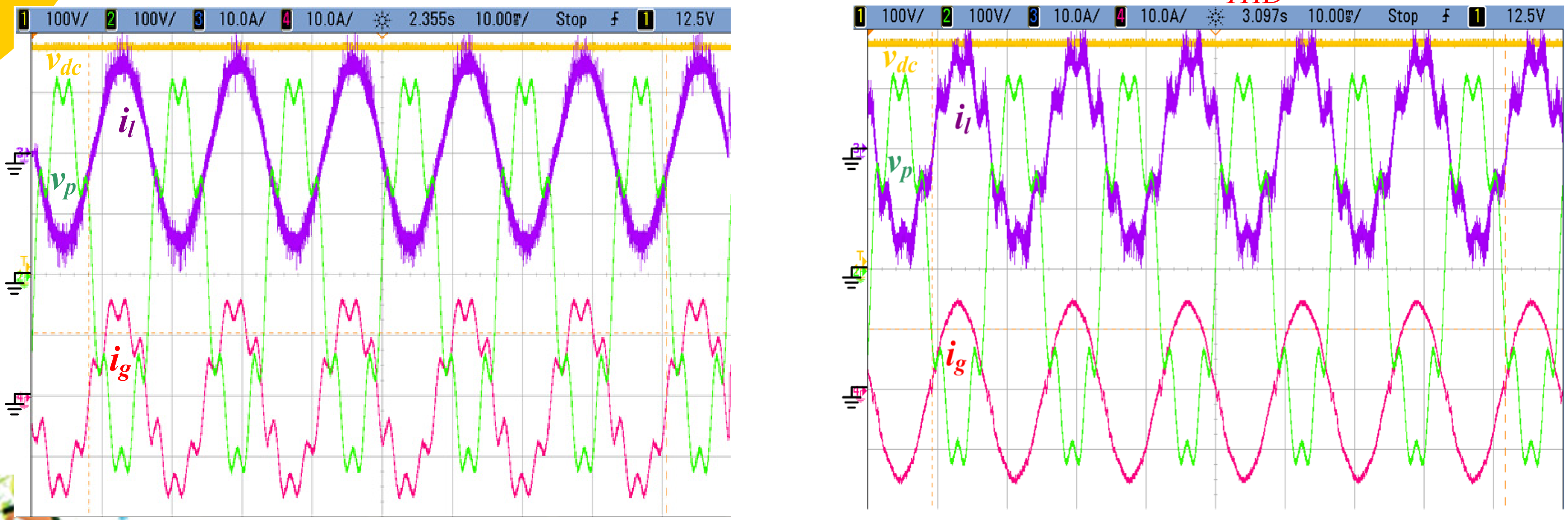
With FCCC I_{THD} : 2.5%

(i_L *and* i_g: 10A/div; v_g *and* v_{dc}: 100v/div; time: 10ms/div)

Experimental Results (Rectification mode) (V_g with harmonics)

- ✓ *Case I:* (V_{THD} : 18.4%)

Harmonic order	%
5	9.8
7	15.8
8	2.16



Without FCCC I_{THD}: 18.7%

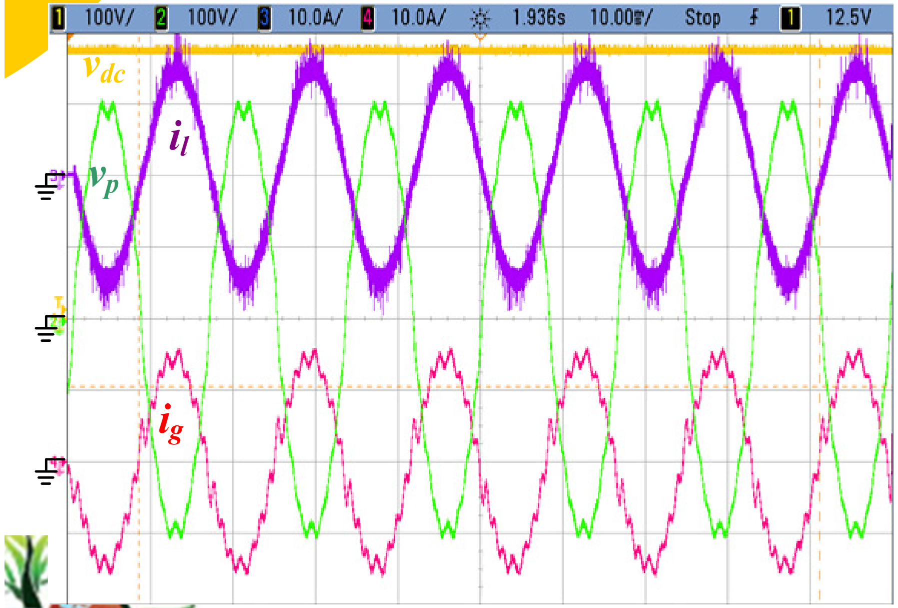
With FCCC I_{THD}: 2.8%

(i_L *and* i_g: 10A/div; v_g *and* v_{dc}: 100v/div; time: 10ms/div)

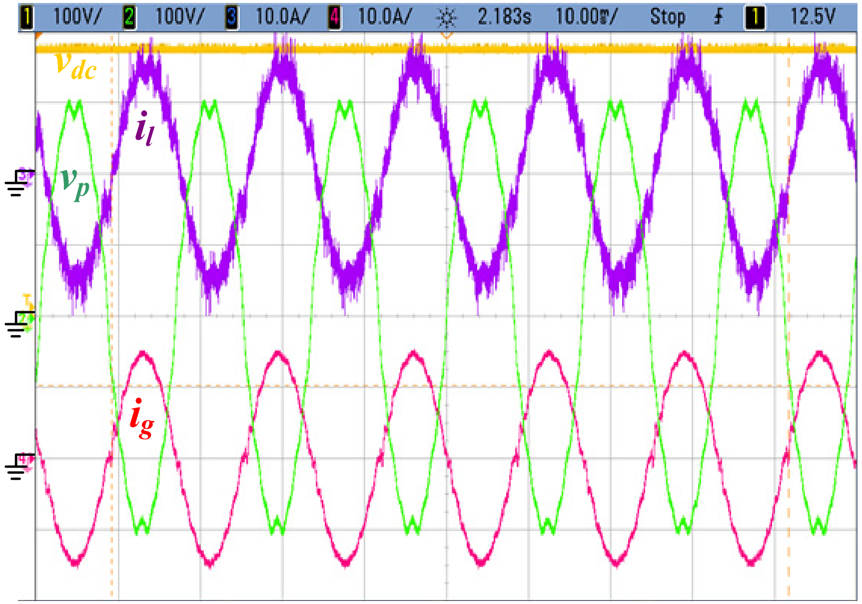
✓ *Case II:* (V_{THD} : 16.4%)

Harmonic order	%	Harmonic order	%
3	4.9	11	1.4
5	1.6	15	2
7	2.7	17	1.1

Without FCCC I_{THD}: 9.3%



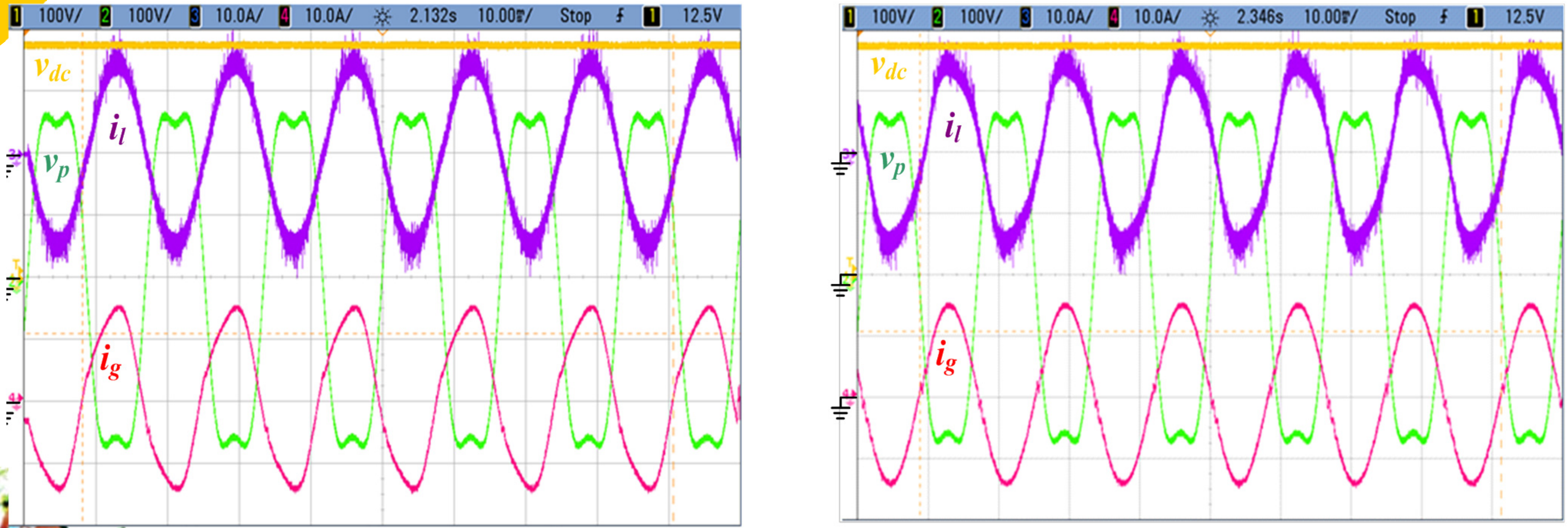
With FCCC I_{THD}: 3.3%



(i_L *and* i_g: 10A/div; v_g *and* v_{dc}: 100v/div; time: 10ms/div)

- ✓ ***Case III:*** (V_{THD} : 17.7%)

Harmonic order	**%**
3	17.8



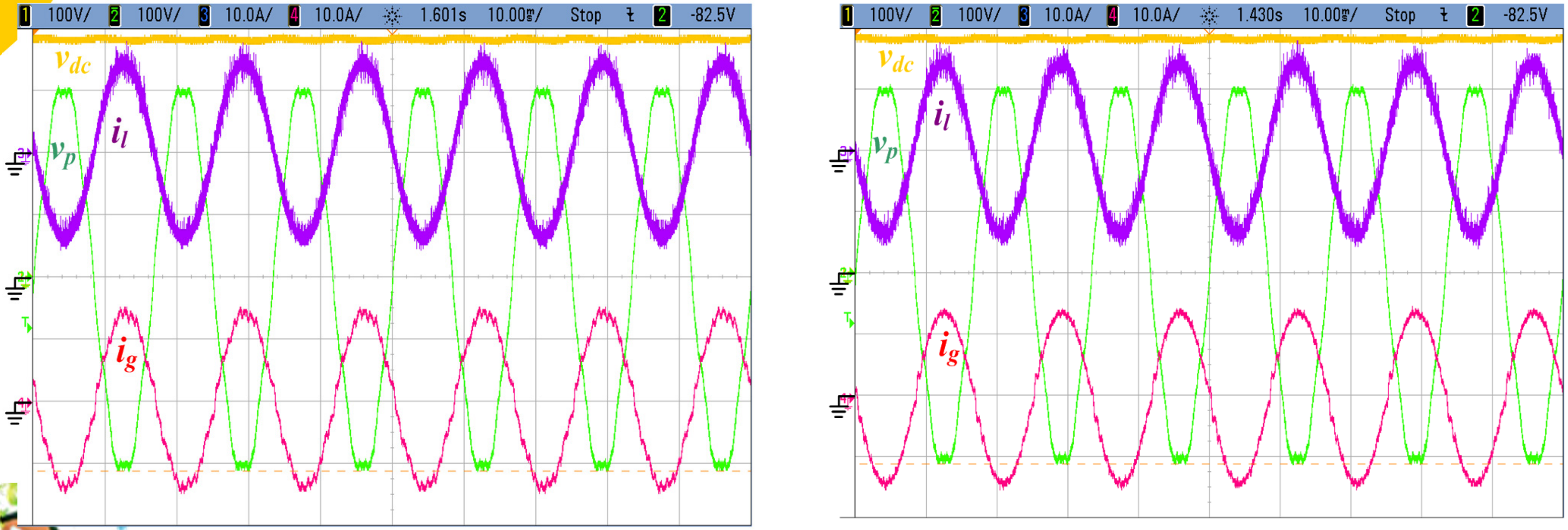
Without FCCC I_{THD}: 17.8%

With FCCC I_{THD} : 2.0%

(i_L *and* i_g: 10A/div; v_g *and* v_{dc}: 100v/div; time: 10ms/div)

- ✓ ***Case IV:*** (V_{THD} : 4.9%)

Harmonic order	%	Harmonic order	%
7	4.6	21	0.9
9	1	39	0.7



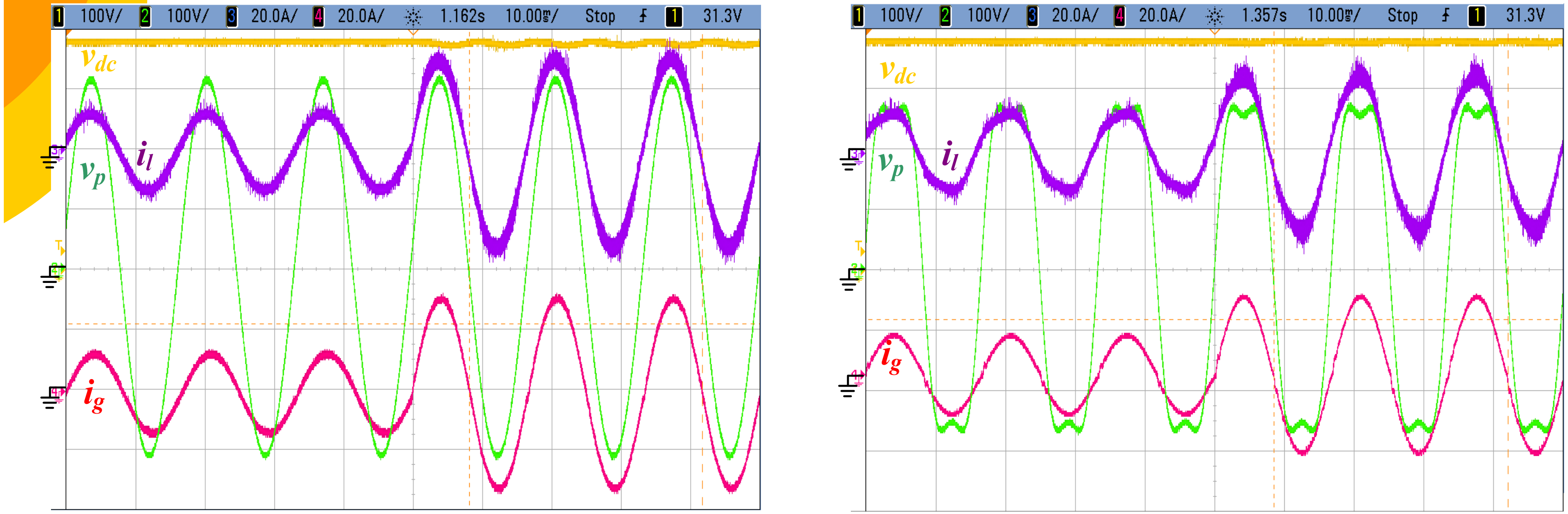
Without FCCC I_{THD}: 5.0%

With FCCC I_{THD} : 2.6%

(i_L *and* i_g: 10A/div; v_g *and* v_{dc}: 100v/div; time: 10ms/div)

Experimental Results (step current change)

10 A → **20 A**



(a) with low-THD v_g

(b) with high-THD v_g

(i_L *and* i_g: 20A/div; v_g *and* v_{dc}: 100v/div; time: 10ms/div)

Conclusions

Four test conditions of grid distortion

Case	Harmonic order	%	Measured Item	Without FCCC (GC Mode)	With FCCC (GC Mode)	Without FCCC (Rect. Mode)	With FCCC (Rect. Mode)
Case I	5	9.8	PF	0.95	0.98	0.95	0.97
	7	15.8	V_{THD}(%)	18.5	18.4	18.4	18.4
	8	2.16	I_{THD}(%)	18.8	3.2	18.7	2.8
Case II	3 5	4.9 1.6	PF	0.98	0.99	0.98	0.99
	7 11	2.7 1.4	V_{THD}(%)	6.4	6.4	6.4	6.4
	15 17	2 1.1	I_{THD}(%)	9.4	3.8	9.3	3.3
Case III	3	17.8	PF	0.95	0.98	0.96	0.97
			V_{THD}(%)	17.8	17.7	17.7	17.8
			I_{THD}(%)	17.7	2.1	17.8	2.0
Case IV	7 9	4.6 1	PF	0.97	0.98	0.97	0.98
	21	0.9	V_{THD}(%)	4.9	5.1	4.9	5.0
	39	0.7	I_{THD}(%)	5.1	2.5	5.1	2.6

1) With D-Σ digital control, the controller can tune loop gains corresponding to inductance variation cycle by cycle.

2) D-Σ digital control can cover wide inductance, dc-bus voltage and line voltage variations, and achieve precise inverter current tracking.

3) With the filter capacitor-current compensation, the grid current can be shaped sinusoidally under distorted grid voltage.

4) D-Σ digital control can improve stability margin, close to 90 °, when injecting current to the grid under high line impedance.

Thanks