High-Order Passive Filters for Grid-Connected Voltage-Source Converters: Topologies and Design Challenges

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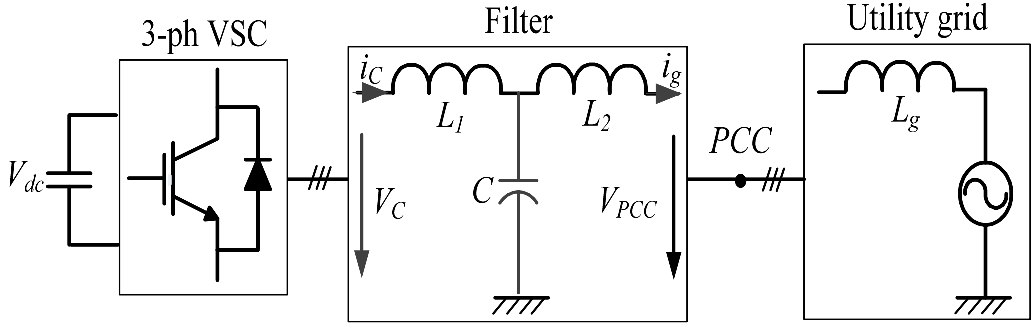
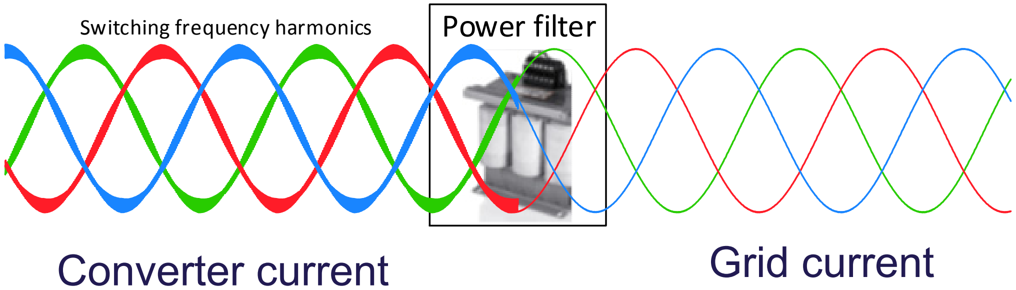
Outline

- Introduction
- Passive Filters Description
- Design Challenges
- Optimum Passive Damping Method
- Conclusions
- Questions

Introduction

- **Power Filters** are needed to link active converters with ideal power sources/loads
- A **high-order** filter is adopted usually due to size and cost considerations
- The aim is to **effectively** filter out the switching harmonics from the active converter and to ensure VSC operation



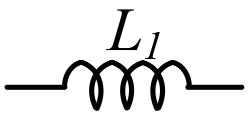


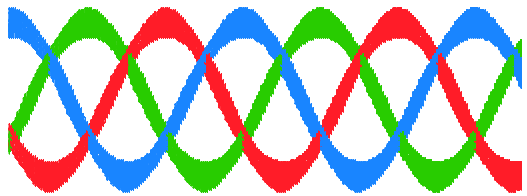
Passive Filters Description

Typical Power Filters

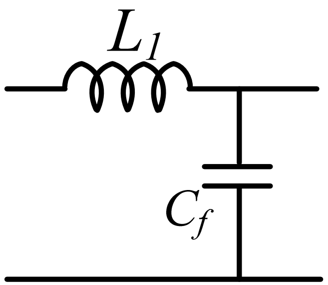
Output current

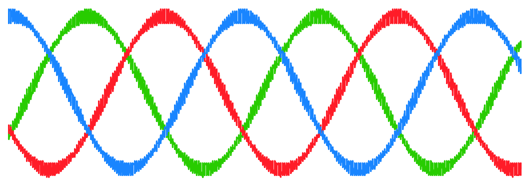
- **L** filter: **20** dB/decade attenuation



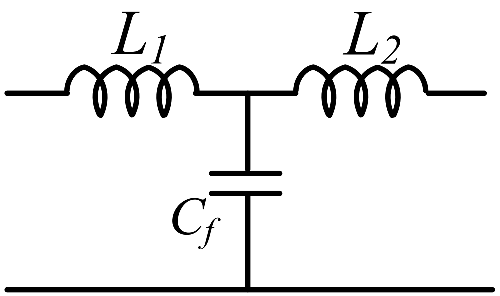


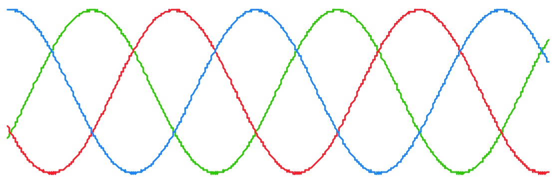
- **LC** filter: **40** dB/decade attenuation





- **LCL** filter: **60** dB/decade attenuation





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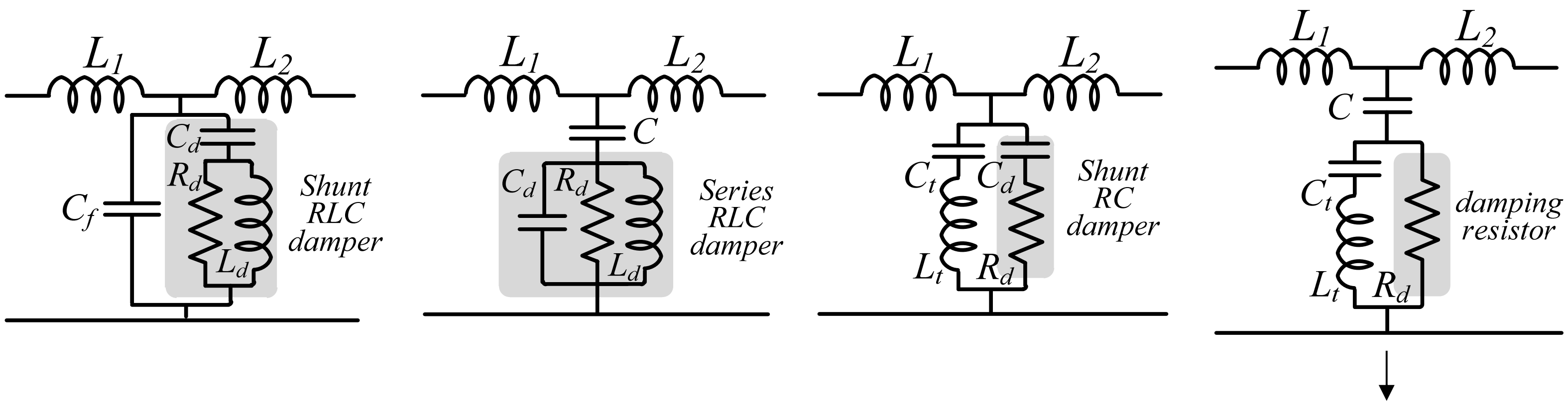
Passive Damped Filters Topologies

- ✓ The key is to ensure high efficiency, low cost and size
- ✓ There should be no risk of harmonic amplification with the utility grid

<u>Shunt passive damped filters topologies</u>

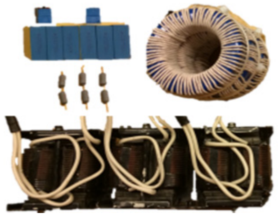


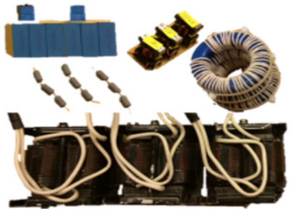
C-type filter used to damp the resonance and the high frequency ripple!*

Beres et al., "Improved Passive Damped LCL Filter to Enhance Stability in Grid-Connected Voltage-Source Converters", Proceedings of CIRED, 2015

Passive Damped Filters Topologies

✓ "More effective" passive filter*





Half physical volume!

Filter	Passive Device	Peak Rating	L/C/R	LI^2 (HA^2)	Volume (cm^3)
LCL + RC	L_1	23 A	1.5 mH	1.06	513
	L_2	21 A	0.7 mH		200
	C_d, C_t	330 V	4.7 µF		22.7
	R_d	17 W	17 Ω		-
Trap + RC	L_1	23 A	1.5 mH	0.89	513
	L_2	21 A	0.3 mH		100
	C_d, C_t	330 V	4.7 µF		22.7
	L_t	3 A	0.05 mH		7.6
	R_d	14 W	13 Ω		-
2traps + RC	L_1	25 A	0.8 mH	0.59	200
	L_2	21 A	0.2 mH		100
	C_d, C_t	330 V	4.7 µF		22.7
	L_t	5 A	0.05 mH		7.6
	C_{t2}	330 V	0.44		3.65
	L_{t2}	2.5 A	0.14 mH		7.6
	R_d	17 W	7.7 Ω		-

$$\frac{L_{Total}}{C_{Total}} = 31$$

$$\frac{L_{Total}}{C_{Total}} = 27$$

$$\frac{L_{Total}}{C_{Total}} = 8.5$$

*Beres et al., "Optimal Design of High-Order Passive-Damped Filters for Grid-Connected Applications ", IEEE Transactions on Power Electronics, Early Access, 2015

Design Challenges of Passive Filters

Known challenges (physical design)

- Size optimized design/reduced filter cost result in low inductances (high capacitance) → high ripple current in the filter → **increased power loss**
- Loss optimized high-order filters results in **increased size** of the filter
- **Accurate models** to optimize the passive filter are **not ready available**

Additional challenges (system level)

- Attenuation of resonance harmonics or limitation of **instabilities risks**
- **Damping is more challenging** for size optimized filters due to increased capacitance
- Harmonics regulations not explicitly defined above 2 kHz (2-9 kHz specifications expected soon)

Design Challenges of Passive Filters

Power Loss in the VSC and Passive Filter

Results from literature

Reference	Frequency range	VSC loss	Filter loss	Core loss calculation method	Verified
[1]	2~6 kHz	0.8~1.5 %	**0.1~0.2 %**	iGSE	–
[2]	2~12 kHz	0.5~1 %	**0.3~0.5 %**	NSE	–
[3]	3~12 kHz	0.5~1.2 %	**1.2~2.2 %**	i^2GSE+loss map	yes

- ~80% of filter loss occurs in the **converter side** inductance!

[1] K. Park, F. Kieferndorf, U. Drofenik, S. Pettersson, and F. Canales, “Weight minimization of LCL filters for high power converters,” in *2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, **2015**, pp. 142–149

[2] L. Wei, Y. Patel, R. Automation, A. Bradley, and W. E. Drive, “Evaluation of LCL Filter Inductor and Active Front End Rectifier Losses Under Different PWM Method,” pp. 3019–3026, **2013**

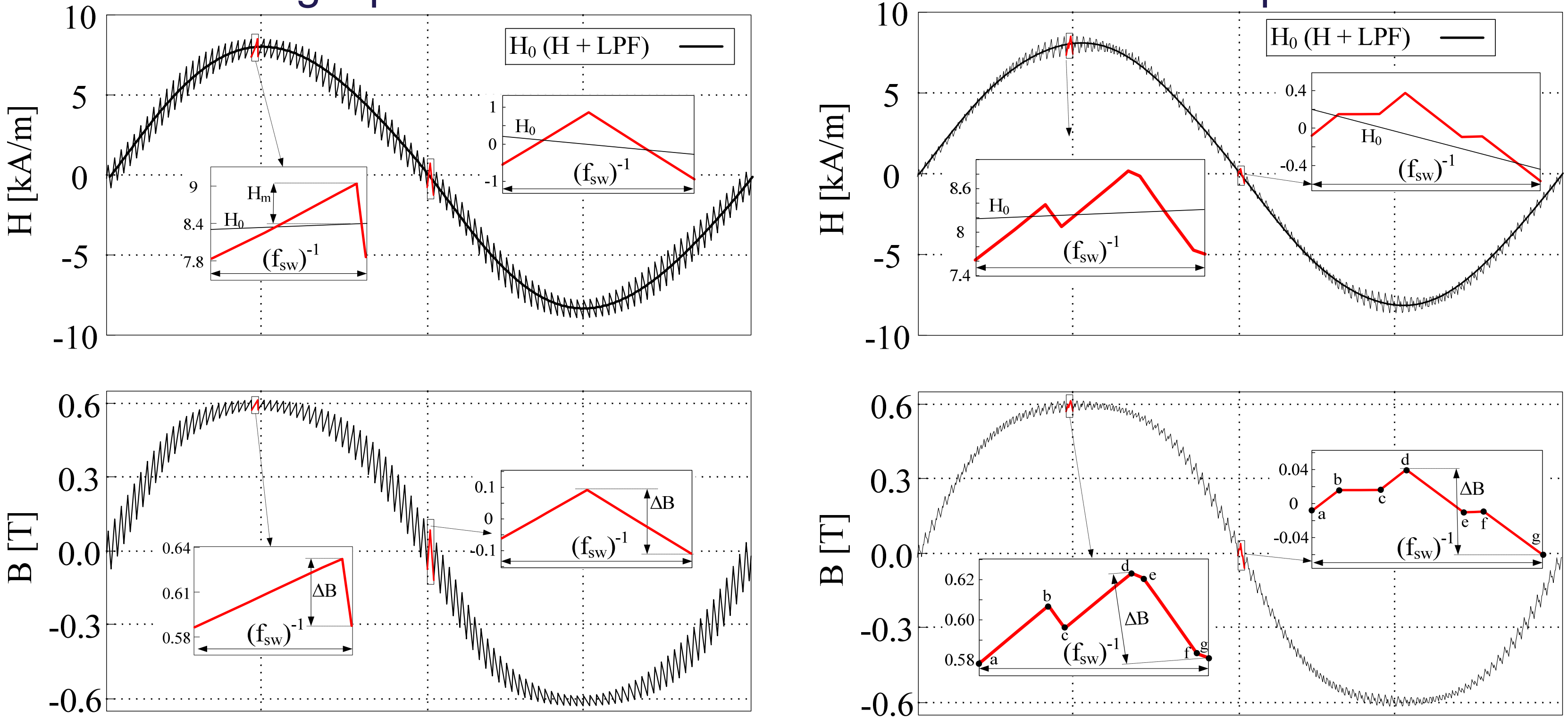
[3] J. Muhlethaler, M. Schweizer, R. Blattmann, J. W. Kolar, and A. Ecklebe, “Optimal Design of LCL Harmonic Filters for Three-Phase PFC Rectifiers,” *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3114–3125, Jul. **2013**

Power Loss in the Converter Side Inductance

Permeability dependence of the Fe-Si material simulated in time-domain

Example: 70% inductance decrease at rated current

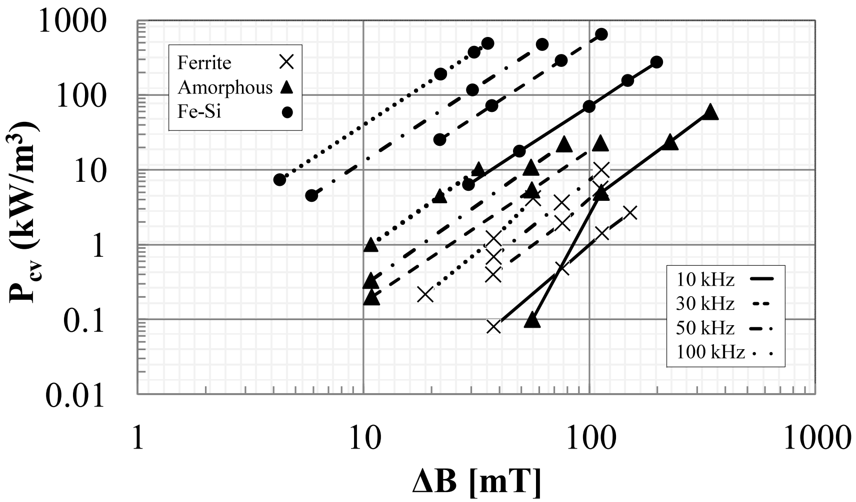
single phase vs three phase



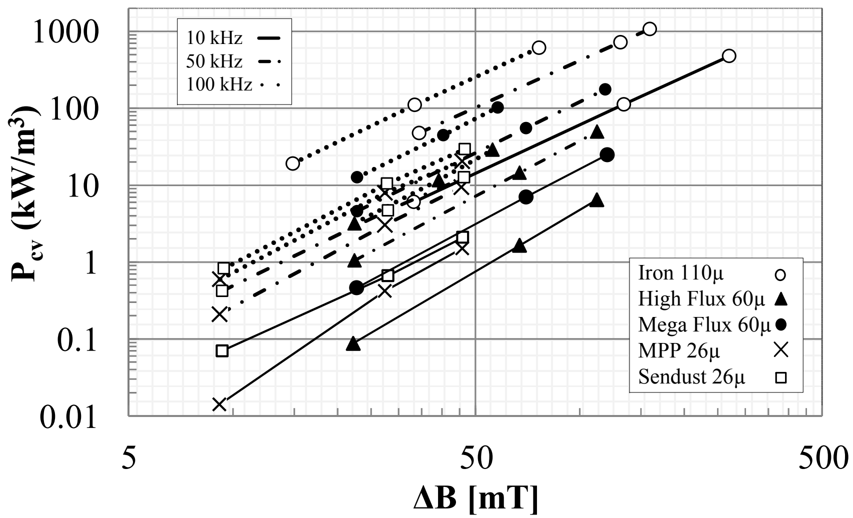
- For a m_i of 0.95, the maximum minor loop frequency is **20 fsw**!

Power Loss in the Converter Side Inductance

- Ferrite + Laminated sheets (H_0=0)



- Powder material (H_0=0)



Core loss of Fe-Si 10 times higher in laminated sheets!

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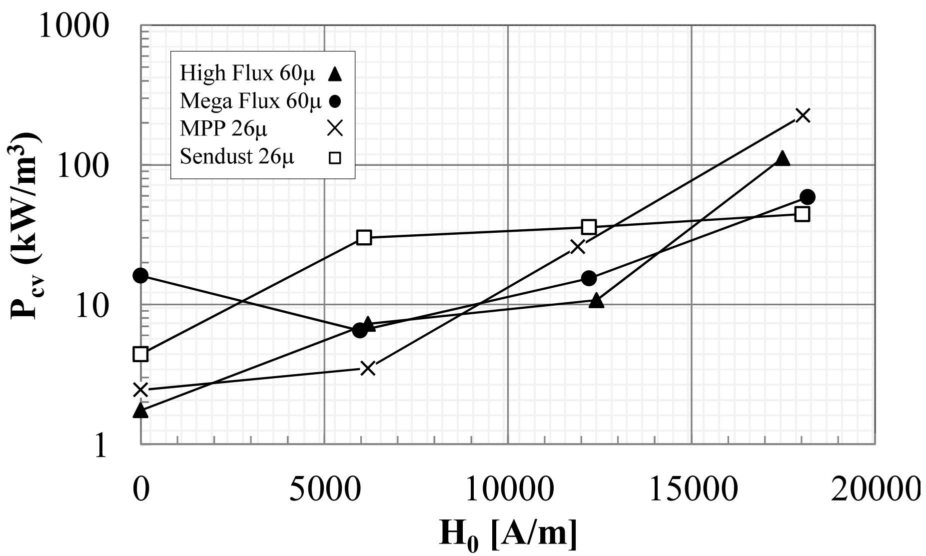
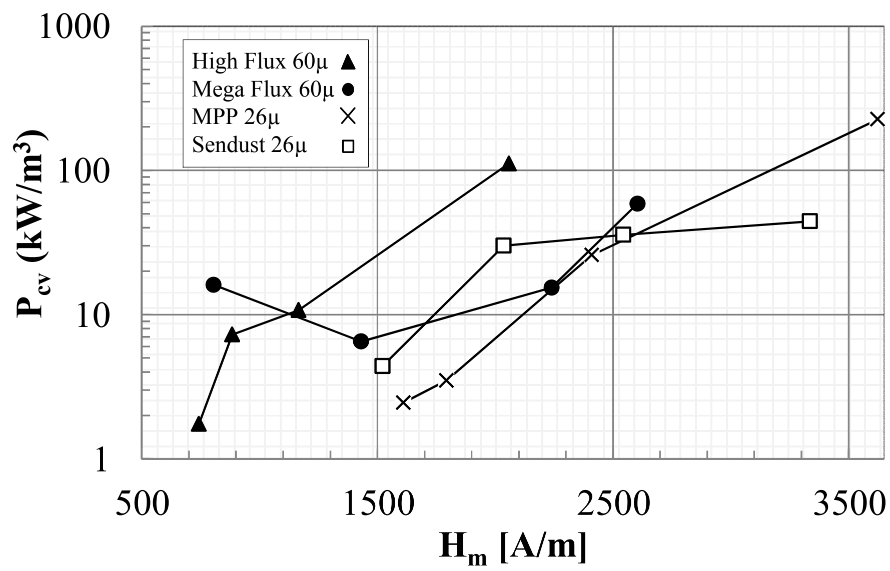
Power Loss in the Converter Side Inductance

- **Inductor loss characterization:**

DC-bias influence at **10 kHz** and **ΔB=0.09T** for powder materials





- Core loss is not always increasing with dc bias!
- Combination of the core loss information and PWM modulation can result in **more significant optimization** of power loss in the filter!

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Current Harmonic Limits

Table I: Individual current harmonic limits at PCC

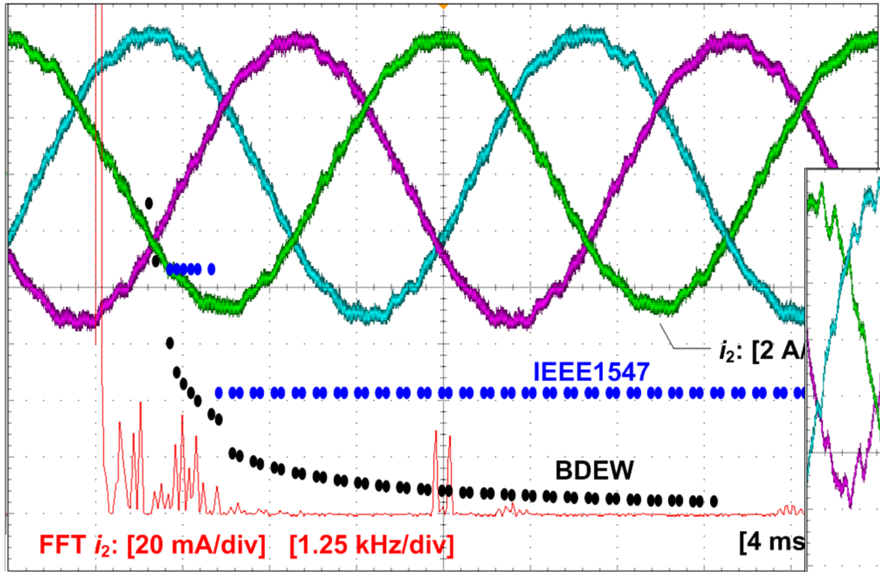
* the limits are referred to the low voltage side of the step-up transformer (400 V)

Harmonic order *h*	VDE-AR-N 4105 (LV)	BDEW (MV)*	IEEE 519 (LV & MV)
5	2.08	2.06	4
7	1.39	2.84	4
11	0.69	1.8	2
13	0.55	1.32	2
17	0.42	0.76	1.5
19	0.35	0.62	1.5
23	0.28	0.42	0.6 $(23 \le h < 35)$
25	0.21	0.35	
$25 < h < 40$	5.2/h	8.67/h	0.3 $(35 \le h < 50)$
$40 < h < 180$	6.24/h	6.24/h	

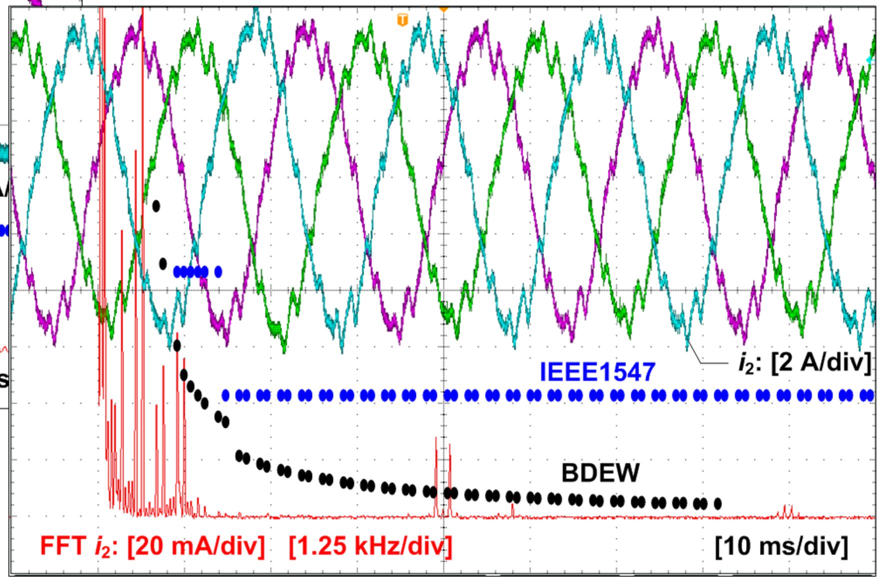
Current Harmonic Limits

LCL filter design according to IEEE 1547 (series R damper)

L_1=4%, L_2=3%, C=10%,R_d =0.3%
P_d=0.4%, K_p=5, K_i=250



L_1=7%, L_2=3%, C=5%, R_d =0.13%,
P_d=0.03%, K_p=8.5, K_i=450

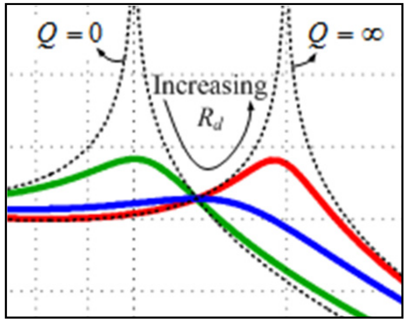


- High difference between different harmonic regulations!
- Presence of low harmonics in the grid current needs compensation!
- Lack of damping can result in harmonics limits exceeded around the resonance!
- Alternative passive damping methods are needed to ensure low damping loss!

Optimum Passive Damping Method

✓ Optimum Damping Parameters

- Damping resistor – used to "limit" resonance instabilities in the utility grid. Low or high values of the resistor have equal impact.
- R.D. Middlebrook develop the "rules" for optimum damping design (1978)
- The damping parameters are dependent on the characteristic parameters of the filter and the ratio(s) between the reactive elements of the filter (capacitors or inductors)*



Resonance frequency can vary in a wide range!

$$R_0, f_0 = f\left(L_{eq}, C_{eq}\right) \qquad a = \frac{L_d}{L_{eq}} \qquad n = \frac{C_d}{C_{eq}}$$

**Beres et al.*, "Optimal Design of High-Order Passive-Damped Filters for Grid-Connected Applications ", IEEE Transactions on Power Electronics, Early Access, 2015

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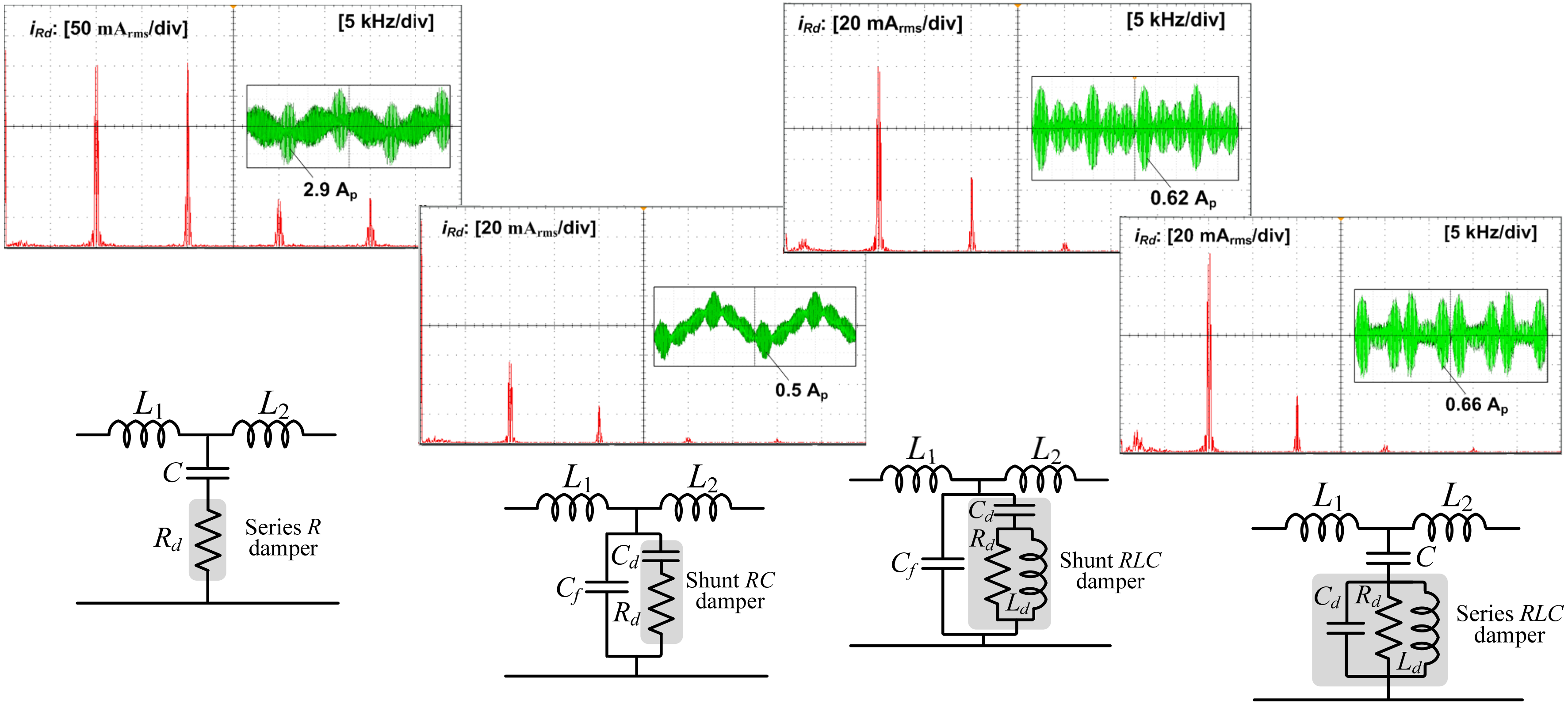
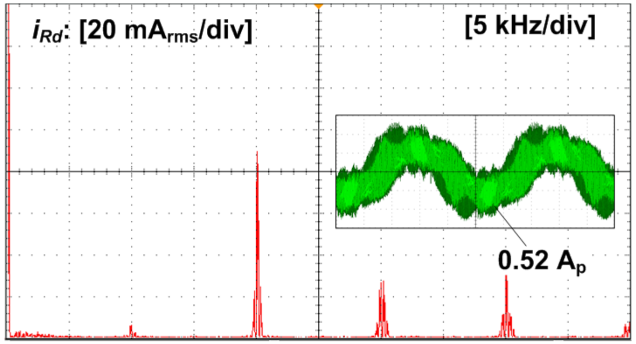
Optimum Passive Damping Method

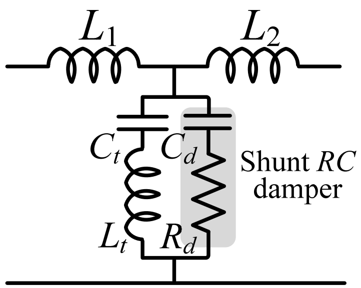
Damping current waveforms

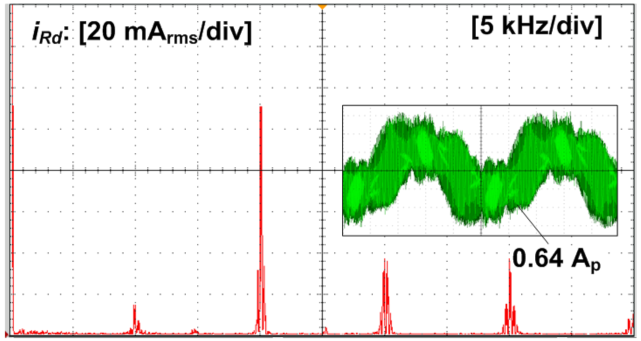


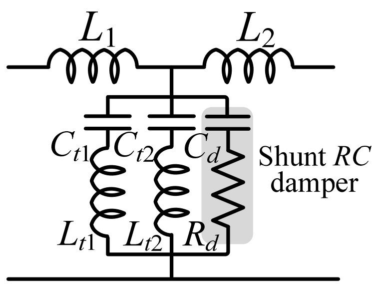
Optimum Passive Damping Method

Damping current waveforms









Half size!

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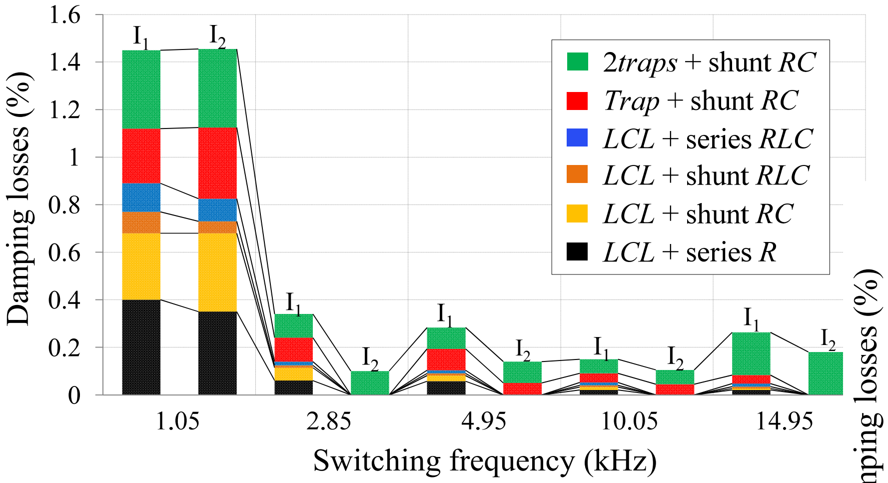
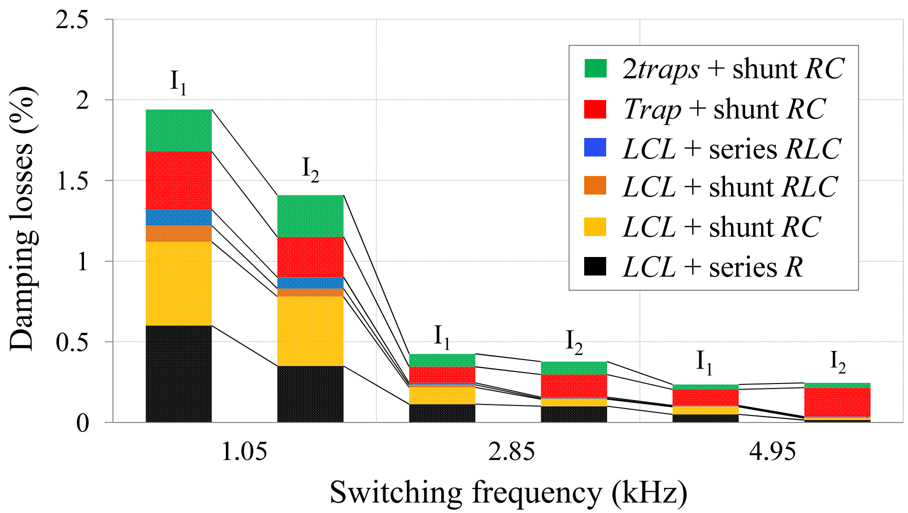
Optimum Passive Damping Method

IEEE 1547 regulations



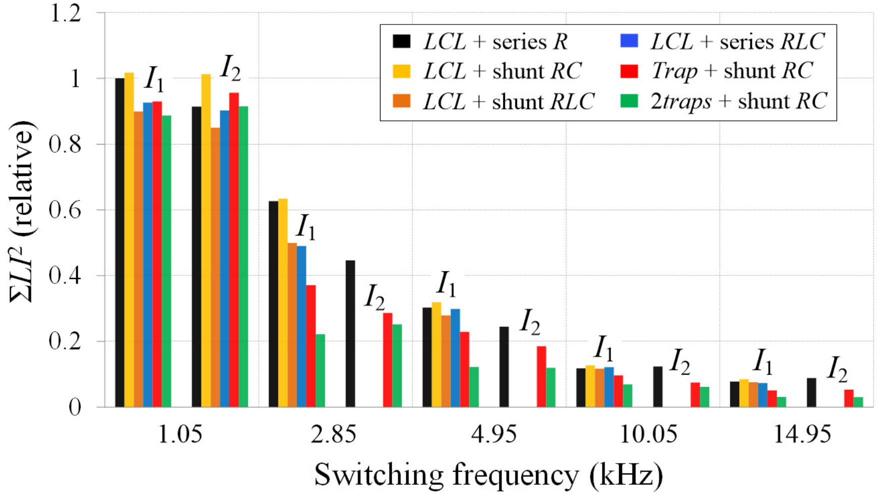
BDEW regulations

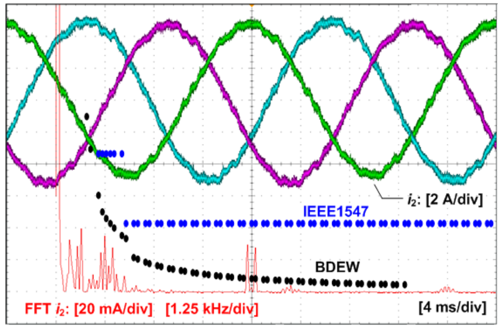


- Passive damping loss are reasonable!
- Very high resonance attenuation requires RLC dampers to limit loss!

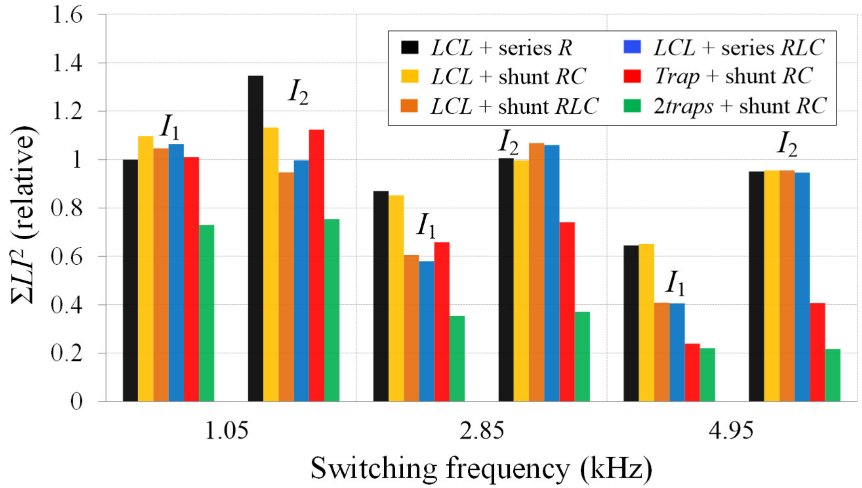
Optimum Passive Damping Method

IEEE 1547 regulations





BDEW regulations



- Design ratings are different depending on harmonic regulations, sensor position or damping topology

Summary

- Latest advancements in power filter topologies for grid connected VSC have been presented
- The optimal design of the filter is related mainly to choice of the **converter side inductance** as function of the VSC topology and VSC specifications
- The **resonance damping** and switching ripple attenuation can be ensured by **shunt passive damped filters**
- An optimum design of the passive damped filters was proposed which can ensure also **low damping loss** and **size**
- Further optimization can be performed by considering:
  - The grid impedance influence on damping and switching harmonics attenuation
  - Harmonization between the PWM method and loss in the converter side inductor

Thank You! Questions?

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